

	L #	Hits	Search Text	DBs
1	L1	181	(result meaning) near10 decod\$3 near10 (instruction command) near20 (depend\$3 based alter\$3 modif\$6 chang\$3 select\$5)	EPO; JPO; DERWENT; IBM_TDB
2	L2	109	1 near20 (value data content memory storage register flag)	EPO; JPO; DERWENT; IBM_TDB
3	L3	681	(result meaning) near10 decod\$3 near10 (instruction command) near20 (depend\$3 based alter\$3 modif\$6 chang\$3 select\$5)	USPAT; US-PGPUB
4	L4	430	3 near20 (value data content memory storage register flag)	USPAT; US-PGPUB
5	L5	120	(result meaning) near10 decod\$3 near10 (instruction command) near20 (depend\$3 based alter\$3 modif\$6 chang\$3)	EPO; JPO; DERWENT; IBM_TDB
6	L8	35	2 not 5	EPO; JPO; DERWENT; IBM_TDB
7	L9	429	(result meaning) near10 decod\$3 near10 (instruction command) near20 (depend\$3 based alter\$3 modif\$6 chang\$3)	USPAT; US-PGPUB
8	L10	163	4 not 9	USPAT; US-PGPUB

	Docum ent ID	U	Title	Current OR
1	JP 20032 49096 A	<input type="checkbox"/>	SEMICONDUCTOR MEMORY DEVICE	
2	JP 20003 47858 A	<input checked="" type="checkbox"/>	MICROPROCESSOR	
3	JP 11212 804 A	<input checked="" type="checkbox"/>	VIRTUAL MACHINE AND PROGRAM CONVERTING DEVICE	
4	JP 11065 839 A	<input checked="" type="checkbox"/>	INSTRUCTION CONTROL MECHANISM OF PROCESSOR	
5	JP 08328 859 A	<input checked="" type="checkbox"/>	VIRTUAL PARALLEL ARITHMETIC UNIT APPLIED TO VLIW COMPUTER	
6	JP 08077 003 A	<input checked="" type="checkbox"/>	DSP PROGRAM PARALLEL PROCESS CONTROLLER	
7	JP 08069 407 A	<input checked="" type="checkbox"/>	PROCESSOR WITH DATA MEMORY	
8	JP 06337 783 A	<input checked="" type="checkbox"/>	PROCESSOR AND METHOD FOR DATA PROCESSING	
9	JP 06030 064 A	<input checked="" type="checkbox"/>	DATA RECEIVER	
10	JP 05341 994 A	<input checked="" type="checkbox"/>	INSTRUCTION PROCESSING SYSTEM AND DATA PROCESSOR	
11	JP 05233 284 A	<input checked="" type="checkbox"/>	INSTRUCTION PREFETCH SYSTEM	
12	JP 05046 384 A	<input checked="" type="checkbox"/>	PIPELINE CONTROL SYSTEM	
13	JP 04054 638 A	<input checked="" type="checkbox"/>	ELECTRONIC COMPUTER	
14	JP 04021 128 A	<input checked="" type="checkbox"/>	INSTRUCTION READING CIRCUIT	
15	JP 03196 348 A	<input checked="" type="checkbox"/>	MEMORY CONTROL CIRCUIT	
16	JP 02118 833 A	<input checked="" type="checkbox"/>	INSTRUCTION DECODER	
17	JP 02019 927 A	<input checked="" type="checkbox"/>	DATA PROCESSOR	
18	JP 01008 457 A	<input checked="" type="checkbox"/>	CONTROL DEVICE FOR STORAGE DEVICE CONSTITUTION	
19	JP 63137 330 A	<input checked="" type="checkbox"/>	MICROPROGRAM CONTROLLER	
20	JP 62186 331 A	<input checked="" type="checkbox"/>	RANDOM NUMBER GENERATING CIRCUIT	
21	JP 62070 954 A	<input checked="" type="checkbox"/>	INFORMATION PROCESSOR	
22	JP 61165 148 A	<input checked="" type="checkbox"/>	TABLE ACCESS INSTRUCTING SYSTEM	

	Docum ent ID	U	Title	Current OR
23	JP 60039 223 A	<input checked="" type="checkbox"/>	MICROCOMPUTER DEVICE	
24	JP 57176 455 A	<input checked="" type="checkbox"/>	MICROPROGRAM CONTROL INFORMATION PROCESSOR	
25	JP 57048 139 A	<input checked="" type="checkbox"/>	MICROPROGRAM CONTROL DEVICE	
26	JP 56147 245 A	<input checked="" type="checkbox"/>	MICROPROGRAM CONTROL DEVICE	
27	JP 56074 751 A	<input checked="" type="checkbox"/>	TEST SYSTEM	
28	EP 12715 51 A2	<input checked="" type="checkbox"/>	Semiconductor memory device and information device	
29	JP 20031 67730 A	<input checked="" type="checkbox"/>	Command set variable microprocessor has programmable logic with command decoder which decodes command to select designated register from register file	
30	EP 12715 51 A	<input checked="" type="checkbox"/>	Semiconductor memory for computer, includes command state machine which decodes input command for controlling either status switching circuit or data switching circuit	
31	CN 13000 05 A	<input checked="" type="checkbox"/>	Data correlation discriminating and selectively transferring circuit for central processor or microcontroller	
32	EP 75623 0 A	<input checked="" type="checkbox"/>	Address setting unit for selecting signal processing instructions in ADPCM system using ROM with conditional branching - has ALU for calculating contents of register file from instruction decoder output for result register, address unit for calculating next instruction ROM address and selector for deciding upon next instruction address	
33	JP 08077 003 A	<input checked="" type="checkbox"/>	DSP program parallel control device for portable telephone - performs parallel execution of instructions of third instruction register within same processing period of second instruction register	
34	US 52127 80 A	<input checked="" type="checkbox"/>	System for single cycle transfer of unmodified data in memory - includes RAM subarrays having odd and even memory locations and data move instruction resulting in externally generated row and column address signals	
35	SU 14447 90 A	<input type="checkbox"/>	Common memory operational elements interface - uses signal to initiate selected current operational element for states memory indication of result destination	

	Docum ent ID	U	Title	Current OR
1	US 20040 02790 2 A1	<input type="checkbox"/>	Semiconductor device with reduced current consumption in standby state	365/222
2	US 20040 02785 7 A1	<input checked="" type="checkbox"/>	Nonvolatile semiconductor memory device allowing high speed data transfer	365/185 .11
3	US 20040 01977 3 A1	<input checked="" type="checkbox"/>	Illegal instruction processing method and processor	712/244
4	US 20040 00668 5 A1	<input checked="" type="checkbox"/>	Processor and instruction control method	712/218
5	US 20040 00490 0 A1	<input checked="" type="checkbox"/>	Semiconductor integrated circuit device with embedded synchronous memory precisely operating in synchronization with high speed clock	365/230 .06
6	US 20030 20238 5 A1	<input checked="" type="checkbox"/>	Method for controlling column decoder enable timing in synchronous semiconductor device and apparatus thereof	365/194
7	US 20030 10133 3 A1	<input checked="" type="checkbox"/>	Data processor	712/226
8	US 20030 09754 1 A1	<input checked="" type="checkbox"/>	Latency tolerant processing equipment	712/1
9	US 20030 09751 9 A1	<input checked="" type="checkbox"/>	Memory subsystem	711/5
10	US 20030 09364 8 A1	<input checked="" type="checkbox"/>	Method and apparatus for interfacing a processor to a coprocessor	712/34
11	US 20030 08427 0 A1	<input checked="" type="checkbox"/>	System and method for translating non-native instructions to native instructions for processing on a host processor	712/204
12	US 20030 07219 9 A1	<input checked="" type="checkbox"/>	Semiconductor memory device	365/200
13	US 20030 05280 2 A1	<input checked="" type="checkbox"/>	Method and apparatus for huffman decoding technique	341/65
14	US 20020 16384 5 A1	<input checked="" type="checkbox"/>	Semiconductor device with reduced current consumption in standby state	365/222
15	US 20020 15827 1 A1	<input checked="" type="checkbox"/>	Semiconductor integrated circuit	257/200
16	US 20020 08785 1 A1	<input checked="" type="checkbox"/>	Microprocessor and an instruction converter	712/239
17	US 20020 08331 3 A1	<input checked="" type="checkbox"/>	Data processing apparatus with many-operand instruction	712/245

	Docum ent ID	U	Title	Current OR
18	US 20020 08271 4 A1	<input checked="" type="checkbox"/>	Processor control apparatus, processor, and processor controlling method	700/1
19	US 20020 08067 7 A1	<input checked="" type="checkbox"/>	Semiconductor memory device	365/233
20	US 20020 07832 5 A1	<input checked="" type="checkbox"/>	Microcomputer and dividing circuit	712/210
21	US 20020 07307 3 A1	<input checked="" type="checkbox"/>	Paralleled content addressable memory search engine	707/2
22	US 20020 04287 1 A1	<input checked="" type="checkbox"/>	DATA PROCESSOR HAVING AN INSTRUCTION DECODER	712/212
23	US 20020 04042 6 A1	<input checked="" type="checkbox"/>	Execution control apparatus of data driven information processor	712/25
24	US 20020 04037 8 A1	<input checked="" type="checkbox"/>	Single instruction multiple data processing	708/232
25	US 20020 02782 3 A1	<input checked="" type="checkbox"/>	Semiconductor memory device	365/230 .03
26	US 20020 02654 5 A1	<input checked="" type="checkbox"/>	Data processing apparatus of high speed process using memory of low speed and low power consumption	710/56
27	US 20010 05414 0 A1	<input checked="" type="checkbox"/>	MICROPROCESSOR INCLUDING AN EFFICIENT IMPLEMENTATION OF EXTREME VALUE INSTRUCTIONS	712/223
28	US 20010 04557 9 A1	<input checked="" type="checkbox"/>	Semiconductor device with reduced current consumption in standby state	257/222
29	US 20010 03351 9 A1	<input checked="" type="checkbox"/>	Semiconductor memory device	365/201
30	US 20010 03229 6 A1	<input checked="" type="checkbox"/>	Data processor	711/128
31	US 66290 99 B2	<input checked="" type="checkbox"/>	Paralleled content addressable memory search engine	707/10
32	US 65976 17 B2	<input checked="" type="checkbox"/>	Semiconductor device with reduced current consumption in standby state	365/222
33	US 65570 98 B2	<input checked="" type="checkbox"/>	Microprocessor including an efficient implementation of extreme value instructions	712/223
34	US 65464 71 B1	<input checked="" type="checkbox"/>	Shared memory multiprocessor performing cache coherency	711/148
35	US 65265 00 B1	<input checked="" type="checkbox"/>	Data driven type information processing system consisting of interconnected data driven type information processing devices	712/25
36	US 65264 74 B1	<input checked="" type="checkbox"/>	Content addressable memory (CAM) with accesses to multiple CAM arrays used to generate result for various matching sizes	711/108

	Docum ent ID	U	Title	Current OR
37	US 65230 54 B1	<input checked="" type="checkbox"/>	Galois field arithmetic processor	708/492
38	US 64626 49 B1	<input checked="" type="checkbox"/>	Air bag failure display system and method	340/435
39	US 64497 07 B1	<input checked="" type="checkbox"/>	Information processing unit, information processing structure unit, information processing structure, memory structure unit and semiconductor memory device	712/14
40	US 64148 94 B2	<input checked="" type="checkbox"/>	Semiconductor device with reduced current consumption in standby state	365/222
41	US 64011 96 B1	<input checked="" type="checkbox"/>	Data processor system having branch control and method thereof	712/241
42	US 63973 23 B1	<input checked="" type="checkbox"/>	Data processor having an instruction decoder	712/212
43	US 63851 04 B2	<input checked="" type="checkbox"/>	Semiconductor memory device having a test mode decision circuit	365/201
44	US 63433 57 B1	<input checked="" type="checkbox"/>	Microcomputer and dividing circuit	712/210
45	US 62955 97 B1	<input checked="" type="checkbox"/>	Apparatus and method for improved vector processing to support extended-length integer arithmetic	712/8
46	US 62826 29 B1	<input checked="" type="checkbox"/>	Pipelined processor for performing parallel instruction recording and register assigning	712/23
47	US 62825 05 B1	<input checked="" type="checkbox"/>	Multi-port memory and a data processor accessing the same	703/25
48	US 62726 20 B1	<input checked="" type="checkbox"/>	Central processing unit having instruction queue of 32-bit length fetching two instructions of 16-bit fixed length in one instruction fetch operation	712/41
49	US 62725 96 B1	<input checked="" type="checkbox"/>	Data processor	711/128
50	US 62667 65 B1	<input checked="" type="checkbox"/>	Computer architecture capable of execution of general purpose multiple instructions	712/215
51	US 62634 23 B1	<input checked="" type="checkbox"/>	System and method for translating non-native instructions to native instructions for processing on a host processor	712/209
52	US 62533 08 B1	<input checked="" type="checkbox"/>	Microcomputer having variable bit width area for displacement and circuit for handling immediate data larger than instruction word	712/210
53	US 62463 88 B1	<input checked="" type="checkbox"/>	Display driving circuit for displaying character on display panel	345/98
54	US 62055 35 B1	<input checked="" type="checkbox"/>	Branch instruction having different field lengths for unconditional and conditional displacements	712/33
55	US 61759 45 B1	<input checked="" type="checkbox"/>	Reed-Solomon decoder	714/784
56	US 61729 18 B1	<input checked="" type="checkbox"/>	Semiconductor memory device allowing high-speed operation of internal data buses	365/189 .11
57	US 61417 46 A	<input checked="" type="checkbox"/>	Information processor	712/214
58	US 61311 54 A	<input checked="" type="checkbox"/>	Microcomputer having variable bit width area for displacement	712/32
59	US 61158 06 A	<input checked="" type="checkbox"/>	Data processor having an instruction decoder and a plurality of executing units for performing a plurality of operations in parallel	712/210

	Docum ent ID	U	Title	Current OR
60	US 61122 99 A	<input checked="" type="checkbox"/>	Method and apparatus to select the next instruction in a superscalar or a very long instruction word computer having N-way branching	712/236
61	US 60887 70 A	<input checked="" type="checkbox"/>	Shared memory multiprocessor performing cache coherency	711/148
62	US 60578 77 A	<input checked="" type="checkbox"/>	NTSC interference detectors using pairs of comb filters with zero-frequency responses, as for DTV receivers	348/21
63	US 60292 44 A	<input checked="" type="checkbox"/>	Microprocessor including an efficient implementation of extreme value instructions	712/223
64	US 60264 85 A	<input checked="" type="checkbox"/>	Instruction folding for a stack-based machine	712/226
65	US 60165 55 A	<input checked="" type="checkbox"/>	Non-intrusive software breakpoints in a processor instruction execution pipeline	714/35
66	US 59918 68 A	<input checked="" type="checkbox"/>	Apparatus and method for processing data with a plurality of flag groups	712/32
67	US 59915 45 A	<input checked="" type="checkbox"/>	Microcomputer having variable bit width area for displacement and circuit for handling immediate data larger than instruction word	712/33
68	US 59833 34 A	<input checked="" type="checkbox"/>	Superscalar microprocessor for out-of-order and concurrently executing at least two RISC instructions translating from in-order CISC instructions	712/23
69	US 59788 22 A	<input checked="" type="checkbox"/>	Circuit for rotating, left shifting, or right shifting bits	708/209
70	US 59745 33 A	<input checked="" type="checkbox"/>	Data processor	712/211
71	US 59699 76 A	<input checked="" type="checkbox"/>	Division circuit and the division method thereof	708/655
72	US 59516 78 A	<input checked="" type="checkbox"/>	Method and apparatus for controlling conditional branch execution in a data processor	712/237
73	US 59480 53 A	<input checked="" type="checkbox"/>	Digital signal processor architecture using signal paths to carry out arithmetic operations	708/522
74	US 59387 59 A	<input checked="" type="checkbox"/>	Processor instruction control mechanism capable of decoding register instructions and immediate instructions with simple configuration	712/209
75	US 59180 45 A	<input checked="" type="checkbox"/>	Data processor and data processing system	712/237
76	US 59095 65 A	<input checked="" type="checkbox"/>	Microprocessor system which efficiently shares register data between a main processor and a coprocessor	712/200
77	US 59039 19 A	<input checked="" type="checkbox"/>	Method and apparatus for selecting a register bank	711/220
78	US 58549 39 A	<input checked="" type="checkbox"/>	Eight-bit microcontroller having a risc architecture	712/41
79	US 58482 68 A	<input checked="" type="checkbox"/>	Data processor with branch target address generating unit	712/233
80	US 58382 49 A	<input checked="" type="checkbox"/>	Control/supervisory signal transmission/reception system	340/3.5 5
81	US 58357 45 A	<input checked="" type="checkbox"/>	Hardware instruction scheduler for short execution unit latencies	712/215
82	US 58288 74 A	<input checked="" type="checkbox"/>	Past-history filtered branch prediction	712/240

	Docum ent ID	U	Title	Current OR
83	US 58092 74 A	<input checked="" type="checkbox"/>	Purge control for ON-chip cache memory	712/210
84	US 57713 63 A	<input checked="" type="checkbox"/>	Single-chip microcomputer having an expandable address area	712/200
85	US 57645 73 A	<input checked="" type="checkbox"/>	Semiconductor device capable of externally and readily identifying set bonding optional function and method of identifying internal function of semiconductor device	365/189 .03
86	US 57614 92 A	<input checked="" type="checkbox"/>	Method and apparatus for uniform and efficient handling of multiple precise events in a processor by including event commands in the instruction set	712/244
87	US 57614 70 A	<input checked="" type="checkbox"/>	Data processor having an instruction decoder and a plurality of executing units for performing a plurality of operations in parallel	712/210
88	US 57520 64 A	<input checked="" type="checkbox"/>	Computer architecture capable of concurrent issuance and execution of general purpose multiple instructions	712/23
89	US 57520 61 A	<input checked="" type="checkbox"/>	Arrangement of data processing system having plural arithmetic logic circuits	712/43
90	US 57519 99 A	<input checked="" type="checkbox"/>	Processor and data memory for outputting and receiving data on different buses for storage in the same location	711/167
91	US 56873 44 A	<input checked="" type="checkbox"/>	Single-chip microcomputer having an expandable address area	711/220
92	US 56825 45 A	<input checked="" type="checkbox"/>	Microcomputer having 16 bit fixed length instruction format	712/41
93	US 56824 91 A	<input checked="" type="checkbox"/>	Selective processing and routing of results among processors controlled by decoding instructions using mask value derived from instruction tag and processor identifier	712/209
94	US 56806 31 A	<input checked="" type="checkbox"/>	Data processor with on-chip cache memory and purge controller responsive to external signal for controlling access to the cache memory	712/207
95	US 56665 10 A	<input checked="" type="checkbox"/>	Data processing device having an expandable address space	711/220
96	US 56492 26 A	<input checked="" type="checkbox"/>	Processor having multiple instruction registers	712/1
97	US 56491 45 A	<input checked="" type="checkbox"/>	Data processor processing a jump instruction	711/213
98	US 56468 75 A	<input checked="" type="checkbox"/>	Denormalization system and method of operation	708/508
99	US 56361 55 A	<input checked="" type="checkbox"/>	Arithmetic processor and arithmetic method	708/631
100	US 56196 66 A	<input checked="" type="checkbox"/>	System for translating non-native instructions to native instructions and combining them into a final bucket for processing on a host processor	712/208
101	US 56196 62 A	<input checked="" type="checkbox"/>	Memory reference tagging	712/216
102	US 56175 50 A	<input checked="" type="checkbox"/>	Data processor generating jump target address of a jump instruction in parallel with decoding of the instruction	712/207
103	US 55926 37 A	<input checked="" type="checkbox"/>	Data processor processing a jump instruction	712/237
104	US 55902 96 A	<input checked="" type="checkbox"/>	Data processor processing a jump instruction	712/229
105	US 55817 19 A	<input checked="" type="checkbox"/>	Multiple block line prediction	712/207



	Docum ent ID	U	Title	Current OR
106	US 55792 53 A	<input checked="" type="checkbox"/>	Computer multiply instruction with a subresult selection option	708/625
107	US 55641 18 A	<input checked="" type="checkbox"/>	Past-history filtered branch prediction	712/240
108	US 55465 52 A	<input checked="" type="checkbox"/>	Method for translating non-native instructions to native instructions and combining them into a final bucket for processing on a host processor	712/209
109	US 55198 41 A	<input checked="" type="checkbox"/>	Multi instruction register mapper	711/202
110	US 55174 62 A	<input checked="" type="checkbox"/>	Synchronous type semiconductor memory device operating in synchronization with an external clock signal	365/233
111	US 54855 87 A	<input checked="" type="checkbox"/>	Data processor calculating branch target address of a branch instruction in parallel with decoding of the instruction	712/234
112	US 54539 27 A	<input checked="" type="checkbox"/>	Data processor for processing branch instructions	712/235
113	US 54407 04 A	<input checked="" type="checkbox"/>	Data processor having branch predicting function	712/239
114	US 54407 02 A	<input checked="" type="checkbox"/>	Data processing system with condition code architecture for executing single instruction range checking and limiting operations	712/223
115	US 54386 68 A	<input checked="" type="checkbox"/>	System and method for extraction, alignment and decoding of CISC instructions into a nano-instruction bucket for execution by a RISC computer	712/204
116	US 54045 52 A	<input checked="" type="checkbox"/>	Pipeline risc processing unit with improved efficiency when handling data dependency	712/41
117	US 54043 38 A	<input checked="" type="checkbox"/>	Synchronous type semiconductor memory device operating in synchronization with an external clock signal	365/233
118	US 53496 72 A	<input checked="" type="checkbox"/>	Data processor having logical address memories and purge capabilities	711/123
119	US 53296 11 A	<input checked="" type="checkbox"/>	Scalable flow virtual learning neurocomputer	706/42
120	US 53218 21 A	<input checked="" type="checkbox"/>	System for processing parameters in instructions of different format to execute the instructions using same microinstructions	712/210
121	US 52993 20 A	<input checked="" type="checkbox"/>	Program control type vector processor for executing a vector pipeline operation for a series of vector data which is in accordance with a vector pipeline	712/231
122	US 52533 49 A	<input checked="" type="checkbox"/>	Decreasing processing time for type 1 dyadic instructions	712/223
123	US 52206 56 A	<input checked="" type="checkbox"/>	System for selecting control parameter for microinstruction execution unit using parameters and parameter selection signal decoded from instruction	712/211
124	US 52127 80 A	<input checked="" type="checkbox"/>	System for single cycle transfer of unmodified data to a next sequentially higher address in a semiconductor memory	365/230 .04
125	US 52069 45 A	<input checked="" type="checkbox"/>	Single-chip pipeline processor for fetching/flushing instruction/data caches in response to first/second hit/mishit signal respectively detected in corresponding to their logical addresses	711/3
126	US 51595 98 A	<input checked="" type="checkbox"/>	Buffer integrated circuit providing testing interface	714/724
127	US 51290 75 A	<input checked="" type="checkbox"/>	Data processor with on-chip logical addressing and off-chip physical addressing	711/169

	Docum ent ID	U	Title	Current OR
128	US 51286 68 A	<input checked="" type="checkbox"/>	Remote-controlled electronic equipment with a transmitting function	340/825 .72
129	US 51173 82 A	<input checked="" type="checkbox"/>	Semiconductor integrated circuit for performing an arithmetic operation including bipolar and MOS transistors	708/490
130	US 51135 03 A	<input checked="" type="checkbox"/>	Data processor providing plural decoders for effecting fast register selection	712/212
131	US 50311 34 A	<input checked="" type="checkbox"/>	System for evaluating multiple integrals	708/444
132	US 49929 38 A	<input checked="" type="checkbox"/>	Instruction control mechanism for a computing system with register renaming, map table and queues indicating available registers	712/217
133	US 49891 40 A	<input checked="" type="checkbox"/>	Single chip pipeline data processor using instruction and operand cache memories for parallel operation of instruction control and executions unit	711/207
134	US 49758 39 A	<input checked="" type="checkbox"/>	Instruction decode method and arrangement suitable for a decoder of microprocessors	712/211
135	US 49126 35 A	<input checked="" type="checkbox"/>	System for reexecuting branch instruction without fetching by storing target instruction control information	712/238
136	US 48976 36 A	<input checked="" type="checkbox"/>	Video display control system for moving display images	345/682
137	US 48688 22 A	<input checked="" type="checkbox"/>	Memory emulation method and system for testing and troubleshooting microprocessor-based electronic systems	714/29
138	US 48581 05 A	<input checked="" type="checkbox"/>	Pipelined data processor capable of decoding and executing plural instructions in parallel	712/235
139	US 48356 79 A	<input checked="" type="checkbox"/>	Microprogram control system	712/212
140	US 48112 03 A	<input checked="" type="checkbox"/>	Hierarchical memory system with separate criteria for replacement and writeback without replacement	711/142
141	US 47899 58 A	<input checked="" type="checkbox"/>	Carry-look-ahead adder including bipolar and MOS transistors	708/710
142	US 47853 93 A	<input checked="" type="checkbox"/>	32-Bit extended function arithmetic-logic unit on a single chip	712/221
143	US 47528 73 A	<input checked="" type="checkbox"/>	Data processor having a plurality of operating units, logical registers, and physical registers for parallel instructions execution	712/23
144	US 47362 88 A	<input checked="" type="checkbox"/>	Data processing device	712/217
145	US 47317 42 A	<input checked="" type="checkbox"/>	Video display control system	345/572
146	US 46301 94 A	<input checked="" type="checkbox"/>	Apparatus for expediting sub-unit and memory communications in a microprocessor implemented data processing system having a multibyte system bus that utilizes a bus command byte	710/100
147	US 45643 02 A	<input checked="" type="checkbox"/>	Control device for printer which has function of format data printing	400/76
148	US 45300 55 A	<input checked="" type="checkbox"/>	Hierarchical memory system with variable regulation and priority of writeback from cache memory to bulk memory	711/136
149	US 45300 54 A	<input checked="" type="checkbox"/>	Processor-addressable timestamp for indicating oldest written-to cache entry not copied back to bulk memory	711/133
150	US 45232 06 A	<input checked="" type="checkbox"/>	Cache/disk system with writeback regulation relative to use of cache memory	711/130

	Docum ent ID	U	Title	Current OR
151	US 44266 46 A	<input checked="" type="checkbox"/>	Self shift type gas discharge panel, driving system	345/62
152	US 43039 78 A	<input checked="" type="checkbox"/>	Integrated-strapdown-air-data sensor system	701/220
153	US RE306 79 E	<input checked="" type="checkbox"/>	Character generating method and system	345/472
154	US 41005 97 A	<input checked="" type="checkbox"/>	Computer controlled distribution apparatus for distributing transactions to and from controlled machine tools having means independent of the computer for completing or stopping a tool function initiated by a computer transaction	700/169
155	US 40694 88 A	<input checked="" type="checkbox"/>	Computer controlled distribution apparatus for distributing transactions to and from controlled machines tools	700/169
156	US 40299 47 A	<input checked="" type="checkbox"/>	Character generating method and system	345/472
157	US 40015 68 A	<input checked="" type="checkbox"/>	Monetary receipt and payment managing apparatus	705/43
158	US 39965 65 A	<input checked="" type="checkbox"/>	Programmable sequence controller	700/9
159	US 38497 65 A	<input checked="" type="checkbox"/>	PROGRAMMABLE LOGIC CONTROLLER	712/246
160	US 37936 31 A	<input checked="" type="checkbox"/>	DIGITAL COMPUTER APPARATUS OPERATIVE WITH JUMP INSTRUCTIONS	712/233
161	US 37532 46 A	<input checked="" type="checkbox"/>	PRINTER ADAPTED FOR OPERATION WITH A PROGRAMMABLE CONTROLLER	358/1.1 5
162	US 36768 46 A	<input checked="" type="checkbox"/>	MESSAGE BUFFERING COMMUNICATION SYSTEM	714/749
163	US 35917 86 A	<input type="checkbox"/>	PREDICTED ITERATION IN DECIMAL DIVISION	708/652

	L #	Hits	Search Text	DBs
1	L1	429	(result meaning) near10 decod\$3 near10 (instruction command) near20 (depend\$3 based alter\$3 modif\$6 chang\$3)	USPAT; US-PGPUB
2	L3	120	(result meaning) near10 decod\$3 near10 (instruction command) near20 (depend\$3 based alter\$3 modif\$6 chang\$3)	EPO; JPO; DERWENT; IBM_TDB
3	L2	260	1 near20 (value data content memory storage register flag)	USPAT; US-PGPUB
4	L5	74	3 near20 (value data content memory storage register flag)	EPO; JPO; DERWENT; IBM_TDB
5	L6	169	1 not 2	USPAT; US-PGPUB
6	L7	46	3 not 5	EPO; JPO; DERWENT; IBM_TDB

	Docum ent ID	U	Title	Current OR
1	JP 20032 42799 A	<input type="checkbox"/>	SEMICONDUCTOR INTEGRATED CIRCUIT	
2	JP 20020 14809 A	<input checked="" type="checkbox"/>	MICROPROCESSOR AND ASSEMBLER AND ITS METHOD AND RECORDING MEDIUM WITH ITS PROGRAM RECORDED	
3	JP 20013 44100 A	<input checked="" type="checkbox"/>	CENTRAL PROCESSING UNIT EQUIPPED WITH PLURAL FLAG REGISTERS	
4	JP 20011 75470 A	<input checked="" type="checkbox"/>	DATA PROCESSOR	
5	JP 20001 37619 A	<input checked="" type="checkbox"/>	MICROCOMPUTER	
6	JP 11177 653 A	<input checked="" type="checkbox"/>	MPEG DATA MSFER CONTROL CIRCUIT	
7	JP 11136 207 A	<input checked="" type="checkbox"/>	RECEPTION SIGNAL CORRECTION SYSTEM AND ORTHOGONAL FREQUENCY DIVISION MULTIPLEX SIGNAL TRANSMITTER	
8	JP 11031 105 A	<input checked="" type="checkbox"/>	DEVICE AND METHOD FOR PRODUCING DATA CAPSULE	
9	JP 11015 590 A	<input checked="" type="checkbox"/>	PERSONAL COMPUTER SYSTEM	
10	JP 10224 147 A	<input checked="" type="checkbox"/>	FREQUENCY-ADJUSTING DEVICE OF OSCILLATOR CIRCUIT	
11	JP 10224 146 A	<input checked="" type="checkbox"/>	FREQUENCY-ADJUSTING DEVICE FOR OSCILLATOR CIRCUIT	
12	JP 10105 396 A	<input checked="" type="checkbox"/>	PROCESSOR	
13	JP 10050 055 A	<input checked="" type="checkbox"/>	SEMICONDUCTOR MEMORY AND DATA PROCESSOR	
14	JP 09311 786 A	<input checked="" type="checkbox"/>	DATA PROCESSOR	
15	JP 08222 996 A	<input checked="" type="checkbox"/>	AUTOMATIC CHANNEL SELECTION METHOD FOR RADIO BROADCAST	
16	JP 08153 000 A	<input checked="" type="checkbox"/>	INSTRUCTION PROCESSOR	
17	JP 07154 677 A	<input checked="" type="checkbox"/>	IMAGE PICKUP DEVICE	
18	JP 06290 078 A	<input checked="" type="checkbox"/>	MICROPROCESSOR	
19	JP 05265 912 A	<input checked="" type="checkbox"/>	COMMAND CODE ISSUING METHOD	
20	JP 05252 119 A	<input checked="" type="checkbox"/>	SAMPLING FREQUENCY CONVERTER	
21	JP 05224 928 A	<input checked="" type="checkbox"/>	DATA PROCESSOR	

	Docum ent ID	U	Title	Current OR
22	JP 05165 629 A	<input checked="" type="checkbox"/>	MICROPROCESSOR	
23	JP 05012 010 A	<input checked="" type="checkbox"/>	BRANCH FORECAST SYSTEM	
24	JP 05012 008 A	<input checked="" type="checkbox"/>	CENTRAL ARITHMETIC PROCESSING UNIT	
25	JP 04353 925 A	<input checked="" type="checkbox"/>	ARITHMETIC UNIT	
26	JP 04328 644 A	<input checked="" type="checkbox"/>	DEBUG BACK-UP DEVICE	
27	JP 04288 688 A	<input checked="" type="checkbox"/>	BIT MAP DISPLAY CONTROLLER	
28	JP 04273 529 A	<input checked="" type="checkbox"/>	PARALLEL ARITHMETIC CIRCUIT	
29	JP 04162 156 A	<input checked="" type="checkbox"/>	INFORMATION PROCESSOR	
30	JP 04062 637 A	<input checked="" type="checkbox"/>	MICROPROCESSOR	
31	JP 04035 180 A	<input checked="" type="checkbox"/>	REPRODUCTION INFORMATION DISPLAY DEVICE	
32	JP 04000 515 A	<input checked="" type="checkbox"/>	CLOCK SUPPLYING SYSTEM AND ARITHMETIC PROCESSOR	
33	JP 03149 622 A	<input checked="" type="checkbox"/>	DATA PROCESSOR	
34	JP 03132 843 A	<input checked="" type="checkbox"/>	MICROPROCESSOR	
35	JP 03095 629 A	<input checked="" type="checkbox"/>	DATA PROCESSOR	
36	JP 01309 129 A	<input checked="" type="checkbox"/>	MICROPROCESSOR	
37	JP 01261 780 A	<input checked="" type="checkbox"/>	STORAGE CONTROL SYSTEM	
38	JP 01106 244 A	<input checked="" type="checkbox"/>	VIRTUAL STORAGE DEVICE	
39	JP 01036 334 A	<input checked="" type="checkbox"/>	MICROCOMPUTER	
40	JP 63208 142 A	<input checked="" type="checkbox"/>	INFORMATION PROCESSOR	
41	JP 63036 432 A	<input checked="" type="checkbox"/>	FLOATING POINT ARITHMETIC UNIT	
42	JP 62285 137 A	<input checked="" type="checkbox"/>	DIGITAL SIGNAL PROCESSOR	
43	JP 62224 828 A	<input checked="" type="checkbox"/>	INFORMATION PROCESSOR	
44	JP 62119 638 A	<input checked="" type="checkbox"/>	DATA PROCESSING SYSTEM	

	Docum ent ID	U	Title	Current OR
45	JP 62044 834 A	<input checked="" type="checkbox"/>	CONTROL SYSTEM FOR ELECTRONIC COMPUTER	
46	JP 60114 972 A	<input checked="" type="checkbox"/>	FORM FORMAT FORMING DEVICE	
47	JP 56074 749 A	<input checked="" type="checkbox"/>	MICROPROGRAM CONTROLLING DEVICE	
48	WO 98137 59 A1	<input checked="" type="checkbox"/>	DATA PROCESSOR AND DATA PROCESSING SYSTEM	
49	JP 20030 85509 A	<input checked="" type="checkbox"/>	Memory card for personal computer, has process unit that detects whether received command is effective, based on decoding result of command and set index value	
50	US 20020 17430 0 A	<input checked="" type="checkbox"/>	Data processor pre-codes advanced instruction portion of instruction data before instruction data is processed and loads instruction codes required for processing into cache memory based on pre-decoding results	
51	EP 11681 29 A	<input checked="" type="checkbox"/>	Microcontroller with variable instruction coding has decoder designed to decode at least one conditional instruction so result of decoding this instruction depends on contents of memory	
52	JP 20013 44100 A	<input checked="" type="checkbox"/>	Central processing unit stores condition of calculation result of decoded input command in several flag registers whose branch conditions are judged based on stored result	
53	JP 20012 65751 A	<input checked="" type="checkbox"/>	Microcomputer device for mobile-communication apparatus, changes operation condition of device based on command data decoding result	
54	WO 20014 2903 A	<input checked="" type="checkbox"/>	Data processing apparatus for executing specific load instruction in which converter circuit converts integer data whose bit length is shorter than bit length of floating-point data register	
55	JP 20011 09626 A	<input checked="" type="checkbox"/>	Pipeline calculating unit in computer system, has instruction decoder decoding instructions published to calculator to store result in downstream latch based on data held by upstream latch	
56	JP 20010 14160 A	<input checked="" type="checkbox"/>	Information processor for pipeline architecture, outputs instruction reading demand to memory based on result of preset instruction decoder	
57	JP 11275 205 A	<input checked="" type="checkbox"/>	Aural command based telephone number dialing system in telephone - has speech recognition unit which recognizes decoded input phonation among stored results and displays best decoding result for dial operation	
58	JP 11232 170 A	<input checked="" type="checkbox"/>	Instruction memory extension apparatus for semiconductor device - has memory control unit for memory operation, based on starting signal and memory extension control unit for memory space based on completion instruction	
59	JP 11191 088 A	<input checked="" type="checkbox"/>	External auxiliary memory for computer system - has two device bus control units which respectively access data unit depending on decoding result from two input output command process units	
60	JP 11154 393 A	<input checked="" type="checkbox"/>	Non-volatile semiconductor memory e.g. electrically erasable programmable read only memory EEPROM, used for recording of multimedia information - has controller which makes predetermined number as designated page unit when predetermined command for designating program unit is included based on decoding result of command decoder	
61	JP 11024 929 A	<input checked="" type="checkbox"/>	Calculation processing apparatus - has selector that chooses one instruction from simultaneously fetched instructions, and outputs chosen instruction to decoder based on decision result of branch conditions about branch instruction	
62	US 58260 97 A	<input checked="" type="checkbox"/>	Data driven information processing - involves subjecting data packets to specified operation processing based on its decoded instruction result and adding operation processing results, cumulatively	

	Docum ent ID	U	Title	Current OR
63	JP 10161 871 A	<input checked="" type="checkbox"/>	Processor architecture e.g. for microprocessor, signal processor - has instruction decoder which outputs control signal to forward data depending on condition judging result, when input instruction is data forwarding instruction	
64	WO 98137 59 A	<input checked="" type="checkbox"/>	Data processor and data processing system - provides task buffers with program storage area and pointer for successively reading out instructions selected through selector, and controls selection by switching controller in accordance with internally or externally-generated event	
65	JP 10050 055 A	<input checked="" type="checkbox"/>	Semiconductor memory for computer system, e.g. SGRAM - has input data controllers which facilitate simultaneous write-in of data in several column addresses of memory cell array based on decoded form of data block write command	
66	JP 08241 296 A	<input checked="" type="checkbox"/>	semiconductor IC with built-in synchronous memory for processing data - has precharge control part which deters generation of precharge demand signal, when first and second prohibition signals show that decoding result is invalid	
67	EP 58299 1 A	<input checked="" type="checkbox"/>	Data processing circuit with CPU and inbuilt electrically rewritable non-volatile flash memory in single substrate - includes command latch made externally writable, command analyser and sequence controller	
68	EP 56127 1 A	<input checked="" type="checkbox"/>	Microcomputer with non-volatile flash memory with writable information - has central processor with multiple memory blocks of different capacities, switched between operation modes when rewriting memory	
69	EP 41701 3 A	<input checked="" type="checkbox"/>	Data processor decoding and executing train of instructions - stores prefetched instruction code, and sequentially outputs instruction with units of set number of bits	
70	SU 16282 15 A	<input checked="" type="checkbox"/>	Transceiver for communication engineering - has signal input of error analyser on transmission side connected to error output of decoder and signal input of matching unit	
71	EP 39976 2 A	<input checked="" type="checkbox"/>	Multiple instruction issue computer architecture - has series of pipeline stages and includes resources for accepting family of instructions at each stage	
72	EP 37437 0 A	<input checked="" type="checkbox"/>	Non exclusive cache lines storage in multiprocessor systems - by allowing instruction execution to continue without result commitment until cache line made exclusive	
73	EP 30122 0 A	<input checked="" type="checkbox"/>	Computer system allowing out of sequence instruction execution - executes instruction register array using processor store and hardware register	
74	SU 11763 34 A	<input type="checkbox"/>	Programmes and micro-programmes tester - has input taken via OR-gates to address counter with output taken to memory and register	



	Docum ent ID	U	Title	Current OR
1	JP 20011 84231 A	<input type="checkbox"/>	PROGRAM DEVELOPMENT SUPPORTING DEVICE AND METHOD OF CONTROLLING THE SAME	
2	JP 20000 99329 A	<input checked="" type="checkbox"/>	PROCESSOR	
3	JP 11283 295 A	<input checked="" type="checkbox"/>	MAGNETIC RECORDING/REPRODUCING DEVICE	
4	JP 11154 393 A	<input checked="" type="checkbox"/>	NON-VOLATILE SEMICONDUCTOR MEMORY	
5	JP 10228 421 A	<input checked="" type="checkbox"/>	MEMORY ACCESS CONTROL CIRCUIT	
6	JP 10164 511 A	<input checked="" type="checkbox"/>	MICROPROCESSOR AND VIDEO INFORMATION PROCESSING SYSTEM	
7	JP 10031 588 A	<input checked="" type="checkbox"/>	ARITHMETIC UNIT AND ITS DESIGNING METHOD	
8	JP 09282 163 A	<input checked="" type="checkbox"/>	DOUBLE INSTRUCTION FETCH PROCESSOR	
9	JP 09172 598 A	<input checked="" type="checkbox"/>	SERVER/CLIENT SYSTEM AND DATA TRANSFER SYSTEM	
10	JP 08095 784 A	<input checked="" type="checkbox"/>	PROCESSOR AND METHOD FOR ARITHMETIC PROCESSING	
11	JP 07250 375 A	<input checked="" type="checkbox"/>	DIGITAL DATA COMMUNICATION ADAPTOR	
12	JP 07154 743 A	<input checked="" type="checkbox"/>	HIGH-SPEED IMAGE REPRODUCING SYSTEM	
13	JP 05268 546 A	<input checked="" type="checkbox"/>	VOICE DECODER CIRCUIT CONTROLLER	
14	JP 05127 892 A	<input checked="" type="checkbox"/>	INSTRUCTION EXECUTING SYSTEM	
15	JP 05066 939 A	<input checked="" type="checkbox"/>	BLOCK OPERATING INSTRUCTION EXECUTING DEVICE FOR INTEGRATED CIRCUIT MICROPROCESSOR	
16	JP 05013 851 A	<input checked="" type="checkbox"/>	LIGHT TRANSMITTING EQUIPMENT	
17	JP 04336 791 A	<input checked="" type="checkbox"/>	ELECTRONIC METER AUTOMATIC INSPECTION SYSTEM	
18	JP 04098 426 A	<input checked="" type="checkbox"/>	MICROPROCESSOR	
19	JP 04054 636 A	<input checked="" type="checkbox"/>	PROCESSOR	
20	JP 03077 137 A	<input checked="" type="checkbox"/>	INFORMATION PROCESSOR	
21	JP 03053 324 A	<input checked="" type="checkbox"/>	PROGRAM LOOP CONTROL SYSTEM	
22	JP 02130 635 A	<input checked="" type="checkbox"/>	SIMULTANEOUS PROCESSING SYSTEM FOR PLURAL INSTRUCTIONS	

	Docum ent ID	U	Title	Current OR
23	JP 63093 036 A	<input checked="" type="checkbox"/>	SECREC Y HOLDING SYSTEM FOR 1-CHIP MICROCOMPUTER	
24	JP 63006 658 A	<input checked="" type="checkbox"/>	FORME SYSTEM	
25	JP 61294 557 A	<input checked="" type="checkbox"/>	INSTRUCTION PROCESSOR	
26	JP 58003 013 A	<input checked="" type="checkbox"/>	CHANNEL CONTROLLING SYSTEM	
27	JP 55049 751 A	<input checked="" type="checkbox"/>	MICROPROGRAM CONTROL UNIT	
28	WO 99211 22 A1	<input checked="" type="checkbox"/>	VOICE-OUTPUT READING SYSTEM WITH GESTURE-BASED NAVIGATION	
29	EP 43720 7 A2	<input checked="" type="checkbox"/>	Information processing system.	
30	EP 41701 3 A2	<input checked="" type="checkbox"/>	Data processor decoding and executing a train of instructions of variable length.	
31	EP 37437 0 A2	<input checked="" type="checkbox"/>	Method for storing into non-exclusive cache lines in multiprocessor systems.	
32	CN 13491 60 A	<input checked="" type="checkbox"/>	Correlation delay eliminating method for streamline control	
33	JP 20020 73328 A	<input checked="" type="checkbox"/>	Digital signal processor judges execution of lower order instruction word, based on the decoding results obtained with respect to previous execution	
34	JP 20010 34471 A	<input checked="" type="checkbox"/>	Very large instruction word system processor used in multimedia fields, executes branch inspection when calculation instruction processing is irrespective of output of instruction decoder	
35	JP 20002 07209 A	<input checked="" type="checkbox"/>	Arithmetic logic unit of very long instruction word processor system, performs various calculations based on decoding result of program and clock supply units respectively supply clock signals for operating ALUs	
36	JP 20001 37619 A	<input checked="" type="checkbox"/>	Signal chip microcomputer consists of instruction decoding circuit which decodes instruction fetched from program memory based on instruction decipherment mode judged by interruption control circuit	
37	US 60584 71 A	<input checked="" type="checkbox"/>	Data processing system includes sub decoder and main decoder which are prevented from decoding instruction other than respective instruction in instruction set.	
38	JP 20000 99329 A	<input checked="" type="checkbox"/>	Processor used for instruction pipeline processing, includes arithmetic logic units which are controlled based on decoded operation indication results	
39	JP 11283 295 A	<input checked="" type="checkbox"/>	Magnetic tape drive speed controller used in VTR - superimposes magnetic tape management information on control signal and decodes it, based on identification result of CTL duty ratio and thereby controls recording command validation	
40	JP 10254 725 A	<input checked="" type="checkbox"/>	Information processor - has rubble circuit which is rearranged when certain predetermined conditions are satisfied by executing instruction	
41	JP 10161 873 A	<input checked="" type="checkbox"/>	Microprocessor with instruction decoding function - performs conditional branch operation based on condition signal depending on execution of instruction prior to conditional branch instruction	
42	US 55600 36 A	<input checked="" type="checkbox"/>	Data processor with emulation function for system debugging - includes operand access control unit, receiving operand data and control values to prevent or permit access to high speed store for operand transfer	

	Docum ent ID	U	Title	Current OR
43	JP 07320 488 A	<input checked="" type="checkbox"/>	Batch erasure method for non-volatile memory device - involves fourth motion doing low speed erasure of small reference threshold voltage according to lump energy of non-volatile element at each erasure	
44	DE 41343 92 A	<input checked="" type="checkbox"/>	parallel processor for several commands - has functional units, commad memory and recall, and decoder for command recognition	
45	EP 43720 7 A	<input checked="" type="checkbox"/>	Information processing system - has execution unit which include flag register and buffer with ALU reading state held in register and buffer	
46	EP 41758 7 A	<input type="checkbox"/>	Data processor with check for undefined addresses - has decoder generating flag for input to detector stage	

	L #	Hits	Search Text	DBs
1	L1	429	(result meaning) near10 decod\$3 near10 (instruction command) near20 (depend\$3 based alter\$3 modif\$6 chang\$3)	USPAT; US-PGPUB
2	L2	260	1 near20 (value data content memory storage register flag)	USPAT; US-PGPUB
3	L3	120	(result meaning) near10 decod\$3 near10 (instruction command) near20 (depend\$3 based alter\$3 modif\$6 chang\$3)	EPO; JPO; DERWENT; IBM_TDB
4	L5	74	3 near20 (value data content memory storage register flag)	EPO; JPO; DERWENT; IBM_TDB

	Docum ent ID	U	Title	Current OR
1	US 20040 02500 0 A1	<input type="checkbox"/>	Multistandard video decoder and decompression system for processing encoded bit streams including start code detection and methods relating thereto	712/300
2	US 20040 01977 5 A1	<input checked="" type="checkbox"/>	Multistandard video decoder and decompression system for processing encoded bit streams including tokens and methods relating thereto	712/300
3	US 20040 01568 0 A1	<input checked="" type="checkbox"/>	Data processor for modifying and executing operation of instruction code	712/226
4	US 20040 00878 8 A1	<input checked="" type="checkbox"/>	MPEG video decoder and MPEG video decoding method	375/240 .25
5	US 20040 00321 4 A1	<input checked="" type="checkbox"/>	Instruction control method and processor	712/234
6	US 20040 00320 7 A1	<input checked="" type="checkbox"/>	Program counter control method and processor	712/218
7	US 20030 22796 9 A1	<input checked="" type="checkbox"/>	Multistandard video decoder and decompression system for processing encoded bit streams including a reconfigurable processing stage and methods relating thereto	375/240 .1
8	US 20030 21485 0 A1	<input checked="" type="checkbox"/>	Non-volatile multi-level semiconductor flash memory device and method of driving same	365/199
9	US 20030 20465 2 A1	<input checked="" type="checkbox"/>	Data transfer control device, electronic equipment and data transfer control method	710/33
10	US 20030 20023 7 A1	<input checked="" type="checkbox"/>	Serial operation pipeline, arithmetic device, arithmetic-logic circuit and operation method using the serial operation pipeline	708/233
11	US 20030 19607 8 A1	<input checked="" type="checkbox"/>	Data pipeline system and data encoding method	712/300
12	US 20030 19159 9 A1	<input checked="" type="checkbox"/>	Method and protocol tester for decoding data encoded in accordance with a protocol description	702/100
13	US 20030 18258 9 A1	<input checked="" type="checkbox"/>	Instruction conversion apparatus and instruction conversion method providing power control information, program and circuit for implementing the instruction conversion, and microprocessor for executing the converted instruction	713/300
14	US 20030 18254 4 A1	<input checked="" type="checkbox"/>	Multistandard video decoder and decompression system for processing encoded bit streams including a decoder with token generator and methods relating thereto	712/300
15	US 20030 17407 7 A1	<input checked="" type="checkbox"/>	Method of performing huffman decoding	341/67
16	US 20030 16360 6 A1	<input checked="" type="checkbox"/>	High-speed memory system	710/1
17	US 20030 15665 2 A1	<input checked="" type="checkbox"/>	Multistandard video decoder and decompression system for processing encoded bit streams including a video formatter and methods relating thereto	375/240 .26

	Docum ent ID	U	Title	Current OR
18	US 20030 15196 2 A1	<input checked="" type="checkbox"/>	Semiconductor integrated circuit device	365/201
19	US 20030 14475 5 A1	<input checked="" type="checkbox"/>	Method for processing and reproducing audio signal at desired sound quality, reduced data volume or adjusted output level, apparatus for processing audio signal with sound quality control information or test tone signal or at reduced data volume, recording medium for recording audio signal with sound quality control information or test tone signal or at reduced data volume, and apparatus for reproducing audio signal at desired sound quality, reduced data volume or adjusted output level	700/94
20	US 20030 14257 0 A1	<input checked="" type="checkbox"/>	Memory controller and serial memory	365/221
21	US 20030 12329 7 A1	<input checked="" type="checkbox"/>	Fast cycle RAM having improved data write operation	365/189 .05
22	US 20030 11784 3 A1	<input checked="" type="checkbox"/>	Non-volatile multi-level semiconductor flash memory device and method of driving same	365/185 .03
23	US 20030 09365 2 A1	<input checked="" type="checkbox"/>	Operand file using pointers and reference counters and a method of use	712/217
24	US 20030 08582 1 A1	<input checked="" type="checkbox"/>	Method of performing Huffman decoding	341/65
25	US 20030 07911 7 A1	<input checked="" type="checkbox"/>	Multistandard video decoder and decompression method for processing encoded bit streams according to respective different standards	712/300
26	US 20030 06601 8 A1	<input checked="" type="checkbox"/>	Apparatus and method for stopping iterative decoding in a CDMA mobile communication system	714/792
27	US 20030 06591 1 A1	<input checked="" type="checkbox"/>	Data processor	712/227
28	US 20030 05608 8 A1	<input checked="" type="checkbox"/>	Processor, compiler and compilation method	712/214
29	US 20030 04367 0 A1	<input checked="" type="checkbox"/>	Memory control apparatus for serial memory	365/221
30	US 20030 04252 3 A1	<input checked="" type="checkbox"/>	Semiconductor integrated circuit device having link element	257/298
31	US 20030 03734 2 A1	<input checked="" type="checkbox"/>	Video encoding scheme supporting the transport of audio and auxiliary information	725/146
32	US 20030 03548 5 A1	<input checked="" type="checkbox"/>	Data separation and decoding device	375/240 .25
33	US 20030 02873 3 A1	<input checked="" type="checkbox"/>	Memory apparatus	711/154

	Docum ent ID	U	Title	Current OR
34	US 20030 02634 2 A1	<input checked="" type="checkbox"/>	Decoding apparatus, decoding method, decoding program, and decoding program storage medium	375/240 .25
35	US 20030 02116 3 A1	<input checked="" type="checkbox"/>	Semiconductor memory device and information device	365/189 .12
36	US 20030 01888 4 A1	<input checked="" type="checkbox"/>	Multistandard video decoder and decompression system for processing encoded bit streams including expanding run length codes and methods relating thereto	712/300
37	US 20030 01655 0 A1	<input checked="" type="checkbox"/>	Semiconductor memory systems, methods, and devices for controlling active termination	365/63
38	US 20030 00501 1 A1	<input checked="" type="checkbox"/>	Sticky z bit	708/490
39	US 20030 00458 8 A1	<input checked="" type="checkbox"/>	Method for processing and reproducing audio signal at desired sound quality, reduced data volume or adjusted output level, apparatus for processing audio signal with sound quality control information or test tone signal or at reduced data volume, recording medium for recording audio signal with sound quality control information or test tone signal or at reduced data volume, and apparatus for reproducing audio signal at desired sound quality, reduced data volume or adjusted output level	700/94
40	US 20020 18689 2 A1	<input checked="" type="checkbox"/>	Method and apparatus for coding of wavelet transformed coefficients	382/240
41	US 20020 17430 0 A1	<input checked="" type="checkbox"/>	Data processor and data processing method	711/123
42	US 20020 15236 9 A1	<input checked="" type="checkbox"/>	Multistandard video decoder and decompression system for processing encoded bit streams including storing data and methods relating thereto	712/300
43	US 20020 12873 9 A1	<input checked="" type="checkbox"/>	Method for processing and reproducing audio signal at desired sound quality, reduced data volume or adjusted output level, apparatus for processing audio signal with sound quality control information or test tone signal or at reduced data volume, recording medium for recording audio signal with sound quality control information or test tone signal or at reduced data volume, and apparatus for reproducing audio signal at desired sound quality, reduced data volume or adjusted output level	700/94
44	US 20020 12381 0 A1	<input checked="" type="checkbox"/>	Method for processing and reproducing audio signal at desired sound quality, reduced data volume or adjusted output level, apparatus for processing audio signal with sound quality control information or test tone signal or at reduced data volume, recording medium for recording audio signal with sound quality control information or test tone signal or at reduced data volume, and apparatus for reproducing audio signal at desired sound quality, reduced data	700/94
45	US 20020 12248 2 A1	<input checked="" type="checkbox"/>	Method of performing video encoding rate control using bit budget	375/240 .03
46	US 20020 11874 6 A1	<input checked="" type="checkbox"/>	Method of performing video encoding rate control using motion estimation	375/240 .03
47	US 20020 08563 3 A1	<input checked="" type="checkbox"/>	Method of performing video encoding rate control	375/240 .03

	Docum ent ID	U	Title	Current OR
48	US 20020 08064 9 A1	<input checked="" type="checkbox"/>	Non-volatile multi-level semiconductor flash memory device and method of driving same	365/185 .03
49	US 20020 07829 4 A1	<input checked="" type="checkbox"/>	HIGH-SPEED RANDOM ACCESS SEMICONDUCTOR MEMORY DEVICE	711/105
50	US 20020 06600 7 A1	<input checked="" type="checkbox"/>	Multistandard video decoder and decompression system for processing encoded bit streams including pipeline processing and methods relating thereto	712/300
51	US 20020 06557 4 A1	<input checked="" type="checkbox"/>	Data processor, semiconductor integrated circuit and CPU	700/121
52	US 20020 04637 2 A1	<input checked="" type="checkbox"/>	SEQUENCE CONTROL CIRCUIT	714/718
53	US 20020 04043 0 A1	<input checked="" type="checkbox"/>	Microcontroller	712/234
54	US 20020 01387 2 A1	<input checked="" type="checkbox"/>	Synchronous signal producing circuit for controlling a data ready signal indicative of end of access to a shared memory and thereby controlling synchronization between processor and coprocessor	710/240
55	US 20020 00267 0 A1	<input checked="" type="checkbox"/>	DATA PROCESSING DEVICE	712/245
56	US 20010 04334 5 A1	<input checked="" type="checkbox"/>	Object optimized printing system and method	358/1.9
57	US 20010 02420 5 A1	<input checked="" type="checkbox"/>	Graphic processor and graphic processing system	345/520
58	US 20010 01309 5 A1	<input checked="" type="checkbox"/>	MICROPROCESSOR HAVING DELAYED INSTRUCTIONS	712/234
59	US 20010 00754 1 A1	<input checked="" type="checkbox"/>	Semiconductor memory device	365/233
60	US 20010 00513 2 A1	<input checked="" type="checkbox"/>	Semiconductor device testing method and system and recording medium	324/158 .1
61	US 20010 00501 2 A1	<input checked="" type="checkbox"/>	Fast cycle ram having improved data write operation	257/1
62	US 20010 00475 6 A1	<input checked="" type="checkbox"/>	Instruction processing apparatus	712/217
63	US 66710 64 B2	<input checked="" type="checkbox"/>	Object optimized printing system and method	358/1.1 5
64	US 66398 63 B2	<input checked="" type="checkbox"/>	Semiconductor integrated circuit device having link element	365/225 .7
65	US 66364 45 B2	<input checked="" type="checkbox"/>	Fast cycle ram having improved data write operation	365/190



	Docum ent ID	U	Title	Current OR
66	US 66287 19 B1	<input checked="" type="checkbox"/>	MPEG video decoder and MPEG video decoding method	375/240 .28
67	US 66178 42 B2	<input checked="" type="checkbox"/>	Semiconductor device testing method and system employing trace data	324/158 .1
68	US 66153 39 B1	<input checked="" type="checkbox"/>	VLIW processor accepting branching to any instruction in an instruction word set to be executed consecutively	712/24
69	US 66088 23 B1	<input checked="" type="checkbox"/>	CDMA mobile communication system and service area	370/331
70	US 66041 93 B1	<input checked="" type="checkbox"/>	Processor in which register number translation is carried out	712/228
71	US 65908 08 B1	<input checked="" type="checkbox"/>	Non-volatile multi-level semiconductor flash memory device and method of driving same	365/185 .03
72	US 65634 39 B1	<input checked="" type="checkbox"/>	Method of performing Huffman decoding	341/65
73	US 65604 97 B2	<input checked="" type="checkbox"/>	METHOD FOR PROCESSING AND REPRODUCING AUDIO SIGNAL AT DESIRED SOUND QUALITY, REDUCED DATA VOLUME OR ADJUSTED OUTPUT LEVEL, APPARATUS FOR PROCESSING AUDIO SIGNAL WITH SOUND QUALITY CONTROL INFORMATION OR TEST TONE SIGNAL OR AT REDUCED DATA VOLUME, RECORDING MEDIUM FOR RECORDING AUDIO SIGNAL WITH SOUND QUALITY CONTROL INFORMATION OR TEST TONE SIGNAL OR AT REDUCED DATA VOLUME, AND APPARATUS FOR REPRODUCING AUDIO SIGNAL AT DESIRED SOUND QUALITY, REDUCED DATA VOLUME OR ADJUSTED OUTPUT LEVEL	700/94
74	US 65494 75 B2	<input checked="" type="checkbox"/>	Semiconductor memory device and information device	365/189 .12
75	US 65393 56 B1	<input checked="" type="checkbox"/>	Signal encoding and decoding method with electronic watermarking	704/270
76	US 65359 84 B1	<input checked="" type="checkbox"/>	Power reduction for multiple-instruction-word processors with proxy NOP instructions	713/320
77	US 65359 72 B1	<input checked="" type="checkbox"/>	Shared dependency checking for status flags	712/217
78	US 65325 30 B1	<input checked="" type="checkbox"/>	Data processing system and method for performing enhanced pipelined operations on instructions for normal and specific functions	712/35
79	US 65163 91 B1	<input checked="" type="checkbox"/>	Multiprocessor system and methods for transmitting memory access transactions for the same	711/146
80	US 65047 89 B2	<input checked="" type="checkbox"/>	Semiconductor memory device	365/233
81	US 65021 86 B2	<input checked="" type="checkbox"/>	Instruction processing apparatus	712/217
82	US 64969 19 B1	<input checked="" type="checkbox"/>	Data processor	712/24
83	US 64964 11 B2	<input checked="" type="checkbox"/>	Non-volatile multi-level semiconductor flash memory device and method of driving same	365/185 .03
84	US 64802 97 B1	<input checked="" type="checkbox"/>	Image forming apparatus	358/1.1 6
85	US 64427 01 B1	<input checked="" type="checkbox"/>	Power saving by disabling memory block access for aligned NOP slots during fetch of multiple instruction words	713/324
86	US 64386 80 B1	<input checked="" type="checkbox"/>	Microprocessor	712/210

	Docum ent ID	U	Title	Current OR
87	US 64357 37 B1	<input checked="" type="checkbox"/>	Data pipeline system and data encoding method	712/200
88	US 64299 48 B1	<input checked="" type="checkbox"/>	Object optimized printing system and method	358/1.1 5
89	US 64272 05 B1	<input checked="" type="checkbox"/>	Digital signal processor and processor reducing the number of instructions upon processing condition execution instructions	712/226
90	US 64250 47 B1	<input checked="" type="checkbox"/>	Process containing address decoders suited to improvements in clock speed	711/101
91	US 64217 73 B1	<input checked="" type="checkbox"/>	Sequence control circuit	712/234
92	US 63850 84 B1	<input checked="" type="checkbox"/>	Semiconductor memory	365/185 .03
93	US 63780 61 B1	<input checked="" type="checkbox"/>	Apparatus for issuing instructions and reissuing a previous instructions by recirculating using the delay circuit	712/200
94	US 63778 62 B1	<input checked="" type="checkbox"/>	Method for processing and reproducing audio signal	700/94
95	US 63565 08 B1	<input checked="" type="checkbox"/>	Semiconductor storage device	365/233
96	US 63358 78 B1	<input checked="" type="checkbox"/>	Non-volatile multi-level semiconductor flash memory device and method of driving same	365/185 .03
97	US 63306 66 B1	<input checked="" type="checkbox"/>	Multistandard video decoder and decompression system for processing encoded bit streams including start codes and methods relating thereto	712/300
98	US 63306 65 B1	<input checked="" type="checkbox"/>	Video parser	712/300
99	US 63270 43 B1	<input checked="" type="checkbox"/>	Object optimized printing system and method	358/1.1 5
100	US 63246 39 B1	<input checked="" type="checkbox"/>	Instruction converting apparatus using parallel execution code	712/212
101	US 62928 63 B1	<input checked="" type="checkbox"/>	PC card	710/313
102	US 62826 33 B1	<input checked="" type="checkbox"/>	High data density RISC processor	712/208
103	US 62826 32 B1	<input checked="" type="checkbox"/>	Information processor having duplicate operation flags	712/42
104	US 62634 22 B1	<input checked="" type="checkbox"/>	Pipeline processing machine with interactive stages operable in response to tokens and system and methods relating thereto	712/209
105	US 62561 04 B1	<input checked="" type="checkbox"/>	Object optimized printing system and method	358/1.1 5
106	US 62398 29 B1	<input checked="" type="checkbox"/>	Systems and methods for object-optimized control of laser power	347/251
107	US 62295 43 B1	<input checked="" type="checkbox"/>	Microprocessor, and graphics processing apparatus and method using the same	345/418
108	US 62197 79 B1	<input checked="" type="checkbox"/>	Constant reconstructing processor which supports reductions in code size	712/210
109	US 61987 67 B1	<input checked="" type="checkbox"/>	Apparatus for color component compression	375/240 .01

	Docum ent ID	U	Title	Current OR
110	US 61700 82 B1	<input checked="" type="checkbox"/>	Taking corrective action in computer programs during instruction processing	717/127
111	US 61669 50 A	<input checked="" type="checkbox"/>	Nonvolatile semiconductor storage device	365/185 .03
112	US 61611 71 A	<input checked="" type="checkbox"/>	Apparatus for pipelining sequential instructions in synchronism with an operation clock	712/42
113	US 61579 97 A	<input checked="" type="checkbox"/>	Processor and information processing apparatus with a reconfigurable circuit	712/226
114	US 61579 96 A	<input checked="" type="checkbox"/>	Processor programably configurable to execute enhanced variable byte length instructions including predicated execution, three operand addressing, and increased register space	712/218
115	US 61579 95 A	<input checked="" type="checkbox"/>	Circuit and method for reducing data dependencies between instructions	712/25
116	US 61311 58 A	<input checked="" type="checkbox"/>	Data processing system capable of executing groups of instructions, including at least one arithmetic instruction, in parallel	712/244
117	US 61120 17 A	<input checked="" type="checkbox"/>	Pipeline processing machine having a plurality of reconfigurable processing stages interconnected by a two-wire interface bus	712/200
118	US 61087 93 A	<input checked="" type="checkbox"/>	Semiconductor device having timing-stabilization circuit and method of testing such semiconductor device	713/400
119	US 60921 83 A	<input checked="" type="checkbox"/>	Data processor for processing a complex instruction by dividing it into executing units	712/215
120	US 60790 09 A	<input checked="" type="checkbox"/>	Coding standard token in a system comprising a plurality of pipeline stages	712/209
121	US 60728 32 A	<input checked="" type="checkbox"/>	Audio/video/computer graphics synchronous reproducing/synthesizing system and method	375/240 .28
122	US 60674 17 A	<input checked="" type="checkbox"/>	Picture start token	712/18
123	US 60584 71 A	<input checked="" type="checkbox"/>	Data processing system capable of executing groups of instructions in parallel	712/212
124	US 60471 12 A	<input checked="" type="checkbox"/>	Technique for initiating processing of a data stream of encoded video information	714/1
125	US 60444 55 A	<input checked="" type="checkbox"/>	Central processing unit adapted for pipeline process	712/213
126	US 60413 87 A	<input checked="" type="checkbox"/>	Apparatus for read/write-access to registers having register file architecture in a central processing unit	711/5
127	US 60383 80 A	<input checked="" type="checkbox"/>	Data pipeline system and data encoding method	712/200
128	US 60351 26 A	<input checked="" type="checkbox"/>	Data pipeline system and data encoding method	712/29
129	US 60264 80 A	<input checked="" type="checkbox"/>	Processor having bug avoidance function and method for avoiding bug in processor	712/37
130	US 60237 57 A	<input checked="" type="checkbox"/>	Data processor	712/209
131	US 60187 76 A	<input checked="" type="checkbox"/>	System for microprogrammable state machine in video parser clearing and resetting processing stages responsive to flush token generating by token generator responsive to received data	710/7

	Docum ent ID	U	Title	Current OR
132	US 60165 43 A	<input checked="" type="checkbox"/>	Microprocessor for controlling the conditional execution of instructions	712/233
133	US 60121 41 A	<input checked="" type="checkbox"/>	Apparatus for detecting and executing traps in a superscalar processor	712/244
134	US 60063 22 A	<input checked="" type="checkbox"/>	Arithmetic logic unit and microprocessor capable of effectively executing processing for specific application	712/200
135	US 60060 13 A	<input checked="" type="checkbox"/>	Object optimized printing system and method	358/1.1 5
136	US 59960 70 A	<input checked="" type="checkbox"/>	Microprocessor capable of executing condition execution instructions using encoded condition execution field in the instructions	712/236
137	US 59785 92 A	<input checked="" type="checkbox"/>	Video decompression and decoding system utilizing control and data tokens	712/1
138	US 59567 41 A	<input checked="" type="checkbox"/>	Interface for connecting a bus to a random access memory using a swing buffer and a buffer manager	711/1
139	US 59565 19 A	<input checked="" type="checkbox"/>	Picture end token in a system comprising a plurality of pipeline stages	712/16
140	US 59419 84 A	<input checked="" type="checkbox"/>	Data processing device	712/218
141	US 59336 51 A	<input checked="" type="checkbox"/>	Programmable controller	712/42
142	US 59336 18 A	<input checked="" type="checkbox"/>	Speculative register storage for storing speculative results corresponding to register updated by a plurality of concurrently recorded instruction	712/217
143	US 59220 69 A	<input checked="" type="checkbox"/>	Reorder buffer which forwards operands independent of storing destination specifiers therein	712/217
144	US 59151 09 A	<input checked="" type="checkbox"/>	Microprocessor for processing a saturation instruction of an optional-bit length value	712/221
145	US 59076 82 A	<input checked="" type="checkbox"/>	Communication LSI for responding to future supplements and modifications of the standard	709/230
146	US 58986 21 A	<input checked="" type="checkbox"/>	Batch erasable single chip nonvolatile memory device and erasing method therefor	365/185 .33
147	US 58929 23 A	<input checked="" type="checkbox"/>	Parallel computer system using properties of messages to route them through an interconnect network and to select virtual channel circuits therewithin	709/239
148	US 58813 01 A	<input checked="" type="checkbox"/>	Inverse modeller	712/1
149	US 58729 89 A	<input checked="" type="checkbox"/>	Processor having a register configuration suited for parallel execution control of loop processing	712/23
150	US 58729 64 A	<input checked="" type="checkbox"/>	Comparison operating unit and graphic operating system	712/234
151	US 58705 80 A	<input checked="" type="checkbox"/>	Decoupled forwarding reorder buffer configured to allocate storage in chunks for instructions having unresolved dependencies	712/218
152	US 58676 96 A	<input checked="" type="checkbox"/>	Saving a program counter value as the return address in an arbitrary general purpose register	712/233
153	US 58600 26 A	<input checked="" type="checkbox"/>	Information processing system for controlling operations of input/output devices of another clusters according to control instructions issued from a cluster	710/33
154	US 58599 26 A	<input checked="" type="checkbox"/>	Device and method for data coding and decoding	382/166

	Docum ent ID	U	Title	Current OR
155	US 58448 43 A	<input checked="" type="checkbox"/>	Single chip data processing apparatus having a flash memory which is rewritable under the control of built-in CPU in the external write mode	365/185 .24
156	US 58420 33 A	<input checked="" type="checkbox"/>	Padding apparatus for passing an arbitrary number of bits through a buffer in a pipeline system	712/1
157	US 58417 31 A	<input checked="" type="checkbox"/>	Semiconductor device having externally settable operation mode	365/233
158	US 58388 96 A	<input checked="" type="checkbox"/>	Central processing unit for preventing program malfunction	714/23
159	US 58357 40 A	<input checked="" type="checkbox"/>	Data pipeline system and data encoding method	712/200
160	US 58156 98 A	<input checked="" type="checkbox"/>	Microprocessor having delayed instructions	712/237
161	US 58128 09 A	<input checked="" type="checkbox"/>	Data processing system capable of execution of plural instructions in parallel	712/212
162	US 58095 52 A	<input checked="" type="checkbox"/>	Data processing system, memory access device and method including selecting the number of pipeline stages based on pipeline conditions	711/169
163	US 58092 70 A	<input checked="" type="checkbox"/>	Inverse quantizer	712/200
164	US 58059 14 A	<input checked="" type="checkbox"/>	Data pipeline system and data encoding method	382/232
165	US 58023 38 A	<input checked="" type="checkbox"/>	Method of self-parallelizing and self-parallelizing multiprocessor using the method	712/217
166	US 57846 31 A	<input checked="" type="checkbox"/>	Huffman decoder	382/246
167	US 57782 08 A	<input checked="" type="checkbox"/>	Flexible pipeline for interlock removal	712/203
168	US 57685 61 A	<input checked="" type="checkbox"/>	Tokens-based adaptive video processing arrangement	710/63
169	US 57649 41 A	<input checked="" type="checkbox"/>	Operating circuit and method for processing signals in ADPCM system	712/209
170	US 57614 90 A	<input checked="" type="checkbox"/>	Changing the meaning of a pre-decode bit in a cache memory depending on branch prediction mode	712/239
171	US 57488 73 A	<input checked="" type="checkbox"/>	Fault recovering system provided in highly reliable computer system having duplicated processors	714/11
172	US 57457 23 A	<input checked="" type="checkbox"/>	Data processing system capable of execution of plural instructions in parallel	712/212
173	US 57370 20 A	<input checked="" type="checkbox"/>	Adaptive field/frame encoding of discrete cosine transform	375/240 .2
174	US 57295 00 A	<input checked="" type="checkbox"/>	Draw with variable internal operation frequency	365/230 .01
175	US 57245 48 A	<input checked="" type="checkbox"/>	System including processor and cache memory and method of controlling the cache memory	711/138
176	US 57245 37 A	<input checked="" type="checkbox"/>	Interface for connecting a bus to a random access memory using a two wire link	711/1
177	US 57154 40 A	<input checked="" type="checkbox"/>	Branch instruction executing device for tracing branch instruments based on instruction type	712/233

	Docum ent ID	U	Title	Current OR
178	US 56921 70 A	<input checked="" type="checkbox"/>	Apparatus for detecting and executing traps in a superscalar processor	712/244
179	US 56873 45 A	<input checked="" type="checkbox"/>	Microcomputer having CPU and built-in flash memory that is rewritable under control of the CPU analyzing a command supplied from an external device	711/103
180	US 56873 03 A	<input checked="" type="checkbox"/>	Printer controller for object optimized printing	358/1.1 8
181	US 56850 10 A	<input checked="" type="checkbox"/>	Data transfer control device for controlling data transfer between shared memories of network clusters	712/28
182	US 56492 29 A	<input checked="" type="checkbox"/>	Pipeline data processor with arithmetic/logic unit capable of performing different kinds of calculations in a pipeline stage	712/24
183	US 56445 04 A	<input checked="" type="checkbox"/>	Dynamically partitionable digital video encoder processor	382/248
184	US 56341 36 A	<input checked="" type="checkbox"/>	Data processor and method of controlling the same	712/237
185	US 56320 23 A	<input checked="" type="checkbox"/>	Superscalar microprocessor including flag operand renaming and forwarding apparatus	712/218
186	US 56280 24 A	<input checked="" type="checkbox"/>	Computer architecture capable of concurrent issuance and execution of general purpose multiple instructions	712/23
187	US 56153 49 A	<input checked="" type="checkbox"/>	Data processing system capable of execution of plural instructions in parallel	712/212
188	US 56030 12 A	<input checked="" type="checkbox"/>	Start code detector	712/208
189	US 55983 68 A	<input checked="" type="checkbox"/>	Batch erasable nonvolatile memory device and erasing method	365/185 .01
190	US 55967 60 A	<input checked="" type="checkbox"/>	Program control method and program control apparatus	712/241
191	US 55817 74 A	<input checked="" type="checkbox"/>	Data processor decoding and executing a train of instructions of variable length at increased speed	712/210
192	US 55795 00 A	<input checked="" type="checkbox"/>	Control apparatus for controlling data read accesses to memory and subsequent address generation scheme based on data/memory width determination and address validation	711/220
193	US 55794 98 A	<input checked="" type="checkbox"/>	Pipelined data processing system capable of stalling and resuming a pipeline operation without using an interrupt processing	712/245
194	US 55399 00 A	<input checked="" type="checkbox"/>	Information processing system	703/26
195	US 55260 54 A	<input checked="" type="checkbox"/>	Apparatus for header generation	348/467
196	US 55240 88 A	<input checked="" type="checkbox"/>	Multi-functional operating circuit providing capability of freely combining operating functions	708/493
197	US 55111 72 A	<input checked="" type="checkbox"/>	Speculative execution processor	712/235
198	US 55069 70 A	<input checked="" type="checkbox"/>	Bus arbitrator circuit	710/113
199	US 54887 10 A	<input checked="" type="checkbox"/>	Cache memory and data processor including instruction length decoding circuitry for simultaneously decoding a plurality of variable length instructions	711/125
200	US 54836 57 A	<input type="checkbox"/>	Method of controlling execution of a data flow program and apparatus therefor	712/27

	Docum ent ID	U	Title	Current OR
1	JP 20032 42799 A	<input type="checkbox"/>	SEMICONDUCTOR INTEGRATED CIRCUIT	
2	JP 20020 14809 A	<input checked="" type="checkbox"/>	MICROPROCESSOR AND ASSEMBLER AND ITS METHOD AND RECORDING MEDIUM WITH ITS PROGRAM RECORDED	
3	JP 20013 44100 A	<input checked="" type="checkbox"/>	CENTRAL PROCESSING UNIT EQUIPPED WITH PLURAL FLAG REGISTERS	
4	JP 20011 75470 A	<input checked="" type="checkbox"/>	DATA PROCESSOR	
5	JP 20001 37619 A	<input checked="" type="checkbox"/>	MICROCOMPUTER	
6	JP 11177 653 A	<input checked="" type="checkbox"/>	MPEG DATA MSFER CONTROL CIRCUIT	
7	JP 11136 207 A	<input checked="" type="checkbox"/>	RECEPTION SIGNAL CORRECTION SYSTEM AND ORTHOGONAL FREQUENCY DIVISION MULTIPLEX SIGNAL TRANSMITTER	
8	JP 11031 105 A	<input checked="" type="checkbox"/>	DEVICE AND METHOD FOR PRODUCING DATA CAPSULE	
9	JP 11015 590 A	<input checked="" type="checkbox"/>	PERSONAL COMPUTER SYSTEM	
10	JP 10224 147 A	<input checked="" type="checkbox"/>	FREQUENCY-ADJUSTING DEVICE OF OSCILLATOR CIRCUIT	
11	JP 10224 146 A	<input checked="" type="checkbox"/>	FREQUENCY-ADJUSTING DEVICE FOR OSCILLATOR CIRCUIT	
12	JP 10105 396 A	<input checked="" type="checkbox"/>	PROCESSOR	
13	JP 10050 055 A	<input checked="" type="checkbox"/>	SEMICONDUCTOR MEMORY AND DATA PROCESSOR	
14	JP 09311 786 A	<input checked="" type="checkbox"/>	DATA PROCESSOR	
15	JP 08222 996 A	<input checked="" type="checkbox"/>	AUTOMATIC CHANNEL SELECTION METHOD FOR RADIO BROADCAST	
16	JP 08153 000 A	<input checked="" type="checkbox"/>	INSTRUCTION PROCESSOR	
17	JP 07154 677 A	<input checked="" type="checkbox"/>	IMAGE PICKUP DEVICE	
18	JP 06290 078 A	<input checked="" type="checkbox"/>	MICROPROCESSOR	
19	JP 05265 912 A	<input checked="" type="checkbox"/>	COMMAND CODE ISSUING METHOD	
20	JP 05252 119 A	<input checked="" type="checkbox"/>	SAMPLING FREQUENCY CONVERTER	
21	JP 05224 928 A	<input checked="" type="checkbox"/>	DATA PROCESSOR	

	Docum ent ID	U	Title	Current OR
22	JP 05165 629 A	<input checked="" type="checkbox"/>	MICROPROCESSOR	
23	JP 05012 010 A	<input checked="" type="checkbox"/>	BRANCH FORECAST SYSTEM	
24	JP 05012 008 A	<input checked="" type="checkbox"/>	CENTRAL ARITHMETIC PROCESSING UNIT	
25	JP 04353 925 A	<input checked="" type="checkbox"/>	ARITHMETIC UNIT	
26	JP 04328 644 A	<input checked="" type="checkbox"/>	DEBUG BACK-UP DEVICE	
27	JP 04288 688 A	<input checked="" type="checkbox"/>	BIT MAP DISPLAY CONTROLLER	
28	JP 04273 529 A	<input checked="" type="checkbox"/>	PARALLEL ARITHMETIC CIRCUIT	
29	JP 04162 156 A	<input checked="" type="checkbox"/>	INFORMATION PROCESSOR	
30	JP 04062 637 A	<input checked="" type="checkbox"/>	MICROPROCESSOR	
31	JP 04035 180 A	<input checked="" type="checkbox"/>	REPRODUCTION INFORMATION DISPLAY DEVICE	
32	JP 04000 515 A	<input checked="" type="checkbox"/>	CLOCK SUPPLYING SYSTEM AND ARITHMETIC PROCESSOR	
33	JP 03149 622 A	<input checked="" type="checkbox"/>	DATA PROCESSOR	
34	JP 03132 843 A	<input checked="" type="checkbox"/>	MICROPROCESSOR	
35	JP 03095 629 A	<input checked="" type="checkbox"/>	DATA PROCESSOR	
36	JP 01309 129 A	<input checked="" type="checkbox"/>	MICROPROCESSOR	
37	JP 01261 780 A	<input checked="" type="checkbox"/>	STORAGE CONTROL SYSTEM	
38	JP 01106 244 A	<input checked="" type="checkbox"/>	VIRTUAL STORAGE DEVICE	
39	JP 01036 334 A	<input checked="" type="checkbox"/>	MICROCOMPUTER	
40	JP 63208 142 A	<input checked="" type="checkbox"/>	INFORMATION PROCESSOR	
41	JP 63036 432 A	<input checked="" type="checkbox"/>	FLOATING POINT ARITHMETIC UNIT	
42	JP 62285 137 A	<input checked="" type="checkbox"/>	DIGITAL SIGNAL PROCESSOR	
43	JP 62224 828 A	<input checked="" type="checkbox"/>	INFORMATION PROCESSOR	
44	JP 62119 638 A	<input checked="" type="checkbox"/>	DATA PROCESSING SYSTEM	



	Docum ent ID	U	Title	Current OR
45	JP 62044 834 A	<input checked="" type="checkbox"/>	CONTROL SYSTEM FOR ELECTRONIC COMPUTER	
46	JP 60114 972 A	<input checked="" type="checkbox"/>	FORM FORMAT FORMING DEVICE	
47	JP 56074 749 A	<input checked="" type="checkbox"/>	MICROPROGRAM CONTROLLING DEVICE	
48	WO 98137 59 A1	<input checked="" type="checkbox"/>	DATA PROCESSOR AND DATA PROCESSING SYSTEM	
49	JP 20030 85509 A	<input checked="" type="checkbox"/>	Memory card for personal computer, has process unit that detects whether received command is effective, based on decoding result of command and set index value	
50	US 20020 17430 0 A	<input checked="" type="checkbox"/>	Data processor pre-codes advanced instruction portion of instruction data before instruction data is processed and loads instruction codes required for processing into cache memory based on pre-decoding results	
51	EP 11681 29 A	<input checked="" type="checkbox"/>	Microcontroller with variable instruction coding has decoder designed to decode at least one conditional instruction so result of decoding this instruction depends on contents of memory	
52	JP 20013 44100 A	<input checked="" type="checkbox"/>	Central processing unit stores condition of calculation result of decoded input command in several flag registers whose branch conditions are judged based on stored result	
53	JP 20012 65751 A	<input checked="" type="checkbox"/>	Microcomputer device for mobile-communication apparatus, changes operation condition of device based on command data decoding result	
54	WO 20014 2903 A	<input checked="" type="checkbox"/>	Data processing apparatus for executing specific load instruction in which converter circuit converts integer data whose bit length is shorter than bit length of floating-point data register	
55	JP 20011 09626 A	<input checked="" type="checkbox"/>	Pipeline calculating unit in computer system, has instruction decoder decoding instructions published to calculator to store result in downstream latch based on data held by upstream latch	
56	JP 20010 14160 A	<input checked="" type="checkbox"/>	Information processor for pipeline architecture, outputs instruction reading demand to memory based on result of preset instruction decoder	
57	JP 11275 205 A	<input checked="" type="checkbox"/>	Aural command based telephone number dialing system in telephone - has speech recognition unit which recognizes decoded input phonation among stored results and displays best decoding result for dial operation	
58	JP 11232 170 A	<input checked="" type="checkbox"/>	Instruction memory extension apparatus for semiconductor device - has memory control unit for memory operation, based on starting signal and memory extension control unit for memory space based on completion instruction	
59	JP 11191 088 A	<input checked="" type="checkbox"/>	External auxiliary memory for computer system - has two device bus control units which respectively access data unit depending on decoding result from two input output command process units	
60	JP 11154 393 A	<input checked="" type="checkbox"/>	Non-volatile semiconductor memory e.g. electrically erasable programmable read only memory EEPROM, used for recording of multimedia information - has controller which makes predetermined number as designated page unit when predetermined command for designating program unit is included based on decoding result of command decoder	
61	JP 11024 929 A	<input checked="" type="checkbox"/>	Calculation processing apparatus - has selector that chooses one instruction from simultaneously fetched instructions, and outputs chosen instruction to decoder based on decision result of branch conditions about branch instruction	
62	US 58260 97 A	<input checked="" type="checkbox"/>	Data driven information processing - involves subjecting data packets to specified operation processing based on its decoded instruction result and adding operation processing results, cumulatively	

	Docum ent ID	U	Title	Current OR
63	JP 10161 871 A	<input checked="" type="checkbox"/>	Processor architecture e.g. for microprocessor, signal processor - has instruction decoder which outputs control signal to forward data depending on condition judging result, when input instruction is data forwarding instruction	
64	WO 98137 59 A	<input checked="" type="checkbox"/>	Data processor and data processing system - provides task buffers with program storage area and pointer for successively reading out instructions selected through selector, and controls selection by switching controller in accordance with internally or externally-generated event	
65	JP 10050 055 A	<input checked="" type="checkbox"/>	Semiconductor memory for computer system, e.g. SGRAM - has input data controllers which facilitate simultaneous write-in of data in several column addresses of memory cell array based on decoded form of data block write command	
66	JP 08241 296 A	<input checked="" type="checkbox"/>	semiconductor IC with built-in synchronous memory for processing data - has precharge control part which deters generation of precharge demand signal, when first and second prohibition signals show that decoding result is invalid	
67	EP 58299 1 A	<input checked="" type="checkbox"/>	Data processing circuit with CPU and inbuilt electrically rewritable non-volatile flash memory in single substrate - includes command latch made externally writable, command analyser and sequence controller	
68	EP 56127 1 A	<input checked="" type="checkbox"/>	Microcomputer with non-volatile flash memory with writable information - has central processor with multiple memory blocks of different capacities, switched between operation modes when rewriting memory	
69	EP 41701 3 A	<input checked="" type="checkbox"/>	Data processor decoding and executing train of instructions - stores prefetched instruction code, and sequentially outputs instruction with units of set number of bits	
70	SU 16282 15 A	<input checked="" type="checkbox"/>	Transceiver for communication engineering - has signal input of error analyser on transmission side connected to error output of decoder and signal input of matching unit	
71	EP 39976 2 A	<input checked="" type="checkbox"/>	Multiple instruction issue computer architecture - has series of pipeline stages and includes resources for accepting family of instructions at each stage	
72	EP 37437 0 A	<input checked="" type="checkbox"/>	Non exclusive cache lines storage in multiprocessor systems - by allowing instruction execution to continue without result commitment until cache line made exclusive	-
73	EP 30122 0 A	<input checked="" type="checkbox"/>	Computer system allowing out of sequence instruction execution - executes instruction register array using processor store and hardware register	
74	SU 11763 34 A	<input type="checkbox"/>	Programmes and micro-programmes tester - has input taken via OR-gates to address counter with output taken to memory and register	

	L #	Hits	Search Text	DBs
1	L1	13	(result meaning) near10 decod\$3 near10 (instruction command) near20 (depend\$3 based alter\$3 modif\$6 chang\$3) near10 mode near10 (flag bit register)	USPAT; US-PGPUB
2	L3	24	decod\$3 near10 (instruction command) near20 (depend\$3 based alter\$3 modif\$6 chang\$3) near10 mode near10 (flag bit register)	EPO; JPO; DERWENT; IBM_TDB
3	L2	91	decod\$3 near10 (instruction command) near20 (depend\$3 based alter\$3 modif\$6 chang\$3) near10 mode near10 (flag bit register)	USPAT; US-PGPUB

	Docum ent ID	U	Title	Current OR
1	JP 20010 35158 A	<input type="checkbox"/>	METHOD AND SYSTEM FOR ACCESSING MEMORY	
2	JP 10171 441 A	<input type="checkbox"/>	CHARACTER DISPLAY CONTROL CIRCUIT	
3	JP 08234 979 A	<input type="checkbox"/>	PROCESSOR HAVING BRANCH INSTRUCTION EXECUTING FUNCTION AND BRANCH INSTRUCTION CONTROL METHOD	
4	JP 04254 985 A	<input type="checkbox"/>	DRAM CONTROLLER	
5	JP 04102 982 A	<input type="checkbox"/>	MICROCOMPUTER	
6	JP 01283 647 A	<input type="checkbox"/>	DUPLICATED ERROR GENERATING DEVICE FOR MICROPROCESSOR	
7	JP 01037 627 A	<input type="checkbox"/>	REGISTER UPDATING MECHANISM	
8	JP 60096 030 A	<input type="checkbox"/>	DECODING SYSTEM	
9	JP 59003 642 A	<input type="checkbox"/>	CONTROL REGISTER PROCESSING SYSTEM	
10	JP 57059 205 A	<input type="checkbox"/>	NUMERIC CONTROLLER	
11	JP 56074 749 A	<input type="checkbox"/>	MICROPROGRAM CONTROLLING DEVICE	
12	DE 19932 465 C1	<input type="checkbox"/>	Arrangement for programming functional devices equipped with digital decoders changes decoder to programming mode using drive voltage on track with digital controller in reset state	
13	EP 10507 98 A1	<input type="checkbox"/>	Decoding instructions	
14	DE 19932 465 C	<input type="checkbox"/>	Arrangement for programming functional devices equipped with digital decoders changes decoder to programming mode using drive voltage on track with digital controller in reset state	
15	EP 10507 98 A	<input type="checkbox"/>	Decode unit for decoding instructions in a processor that can support three instruction modes has detector that temporarily allows first length instructions to be decoded without changing instruction mode held in register	
16	US 60121 38 A	<input type="checkbox"/>	Dynamically variable length CPU pipeline for executing multiple instruction sets	
17	JP 11154 393 A	<input type="checkbox"/>	Non-volatile semiconductor memory e.g. electrically erasable programmable read only memory EEPROM, used for recording of multimedia information - has controller which makes predetermined number as designated page unit when predetermined command for designating program unit is included based on decoding result of command decoder	
18	US 58023 60 A	<input type="checkbox"/>	Integrated circuit with digital processor for dynamic selection of instruction execution intervals - has decode stage coupled to execute stage with mode input for selecting number of clock cycles taken to execute flag-modifying instruction	
19	US 51230 96 A	<input type="checkbox"/>	Data processor with addressing mode decoding function - modifies entry address of microinstruction when addressing mode of operand detected to enable entry address	
20	JP 02011 076 A	<input type="checkbox"/>	Sound decoder for MUSE television receiver - operates muting circuit when state change of mode command bit in control code is detected NoAbstract Dwg 0/2	

	Docum ent ID	U	Title	Current OR
21	DE 35007 41 A	<input type="checkbox"/>	Integrated circuit for floppy disc drive control - has registers to handle control and data transfers between disc drive and computer operating with status interlock stage	
22	SU 10658 52 A	<input type="checkbox"/>	Multi-computer network computer interfacing unit - has memory data input coupled through high-way with coupling amplifier data outputs to group lines	
23	WO 83030 17 A	<input type="checkbox"/>	Computer with static cache - automatically maps memory contents into machine registers during program execution	
24	EP 40703 A	<input type="checkbox"/>	Enhancement of 370 type data processor - reduces overhead incurred by multiple users by permitting program in one address space to obtain access to data in another address space	

	Docum ent ID	U	Title	Current OR
1	US 20030 02116 3 A1	<input type="checkbox"/>	Semiconductor memory device and information device	365/189 .12
2	US 20010 00754 1 A1	<input type="checkbox"/>	Semiconductor memory device	365/233
3	US 20010 00513 2 A1	<input type="checkbox"/>	Semiconductor device testing method and system and recording medium	324/158 .1
4	US 66178 42 B2	<input type="checkbox"/>	Semiconductor device testing method and system employing trace data	324/158 .1
5	US 65494 75 B2	<input type="checkbox"/>	Semiconductor memory device and information device	365/189 .12
6	US 65047 89 B2	<input type="checkbox"/>	Semiconductor memory device	365/233
7	US 64250 47 B1	<input type="checkbox"/>	Process containing address decoders suited to improvements in clock speed	711/101
8	US 57614 90 A	<input type="checkbox"/>	Changing the meaning of a pre-decode bit in a cache memory depending on branch prediction mode	712/239
9	US 55069 70 A	<input type="checkbox"/>	Bus arbitrator circuit	710/113
10	US 54127 84 A	<input type="checkbox"/>	Apparatus for parallelizing serial instruction sequences and creating entry points into parallelized instruction sequences at places other than beginning of particular parallelized instruction sequence	712/245
11	US 54086 58 A	<input type="checkbox"/>	Self-scheduling parallel computer system and method	712/216
12	US 53476 39 A	<input type="checkbox"/>	Self-parallelizing computer system and method	712/203
13	US 44146 22 A	<input type="checkbox"/>	Addressing system for a computer, including a mode register	711/215

	Docum ent ID	U	Title	Current OR
1	US 20040 01975 6 A1	<input type="checkbox"/>	Memory device supporting a dynamically configurable core organization	711/170
2	US 20030 22329 3 A1	<input checked="" type="checkbox"/>	Synchronous type semiconductor memory device	365/200
3	US 20030 16451 0 A1	<input checked="" type="checkbox"/>	Redundancy architecture for repairing semiconductor memories	257/200
4	US 20030 13577 9 A1	<input checked="" type="checkbox"/>	Microprocessor	713/600
5	US 20030 12652 9 A1	<input checked="" type="checkbox"/>	Wafer burn-in test mode circuit	714/720
6	US 20030 10133 3 A1	<input checked="" type="checkbox"/>	Data processor	712/226
7	US 20030 08573 1 A1	<input checked="" type="checkbox"/>	Semiconductor device having test mode entry circuit	326/16
8	US 20030 08149 1 A1	<input checked="" type="checkbox"/>	SEMICONDUCTOR MEMORY DEVICE WITH REDUCED POWER CONSUMPTION	365/233
9	US 20030 07578 9 A1	<input checked="" type="checkbox"/>	Semiconductor storage device having memory chips in a stacked structure	257/678
10	US 20030 06153 6 A1	<input checked="" type="checkbox"/>	Power controlling method for semiconductor storage device and semiconductor storage device employing same	714/14
11	US 20030 02116 3 A1	<input type="checkbox"/>	Semiconductor memory device and information device	365/189 .12
12	US 20030 01445 7 A1	<input checked="" type="checkbox"/>	Method and apparatus for vector processing	708/520
13	US 20020 17107 5 A1	<input checked="" type="checkbox"/>	Register setting method and semiconductor device	257/10
14	US 20020 14592 9 A1	<input checked="" type="checkbox"/>	Control circuit and semiconductor memory device	365/222
15	US 20010 02342 4 A1	<input checked="" type="checkbox"/>	Exponent unit of data processing system	708/277
16	US 20010 00754 1 A1	<input type="checkbox"/>	Semiconductor memory device	365/233
17	US 20010 00513 2 A1	<input type="checkbox"/>	Semiconductor device testing method and system and recording medium	324/158 .1

	Docum ent ID	U	Title	Current OR
18	US 66788 18 B1	<input checked="" type="checkbox"/>	Decoding next instruction of different length without length mode indicator change upon length change instruction detection	712/210
19	US 66752 90 B1	<input checked="" type="checkbox"/>	Processor for improving instruction utilization using multiple parallel processors and computer system equipped with the processor	712/229
20	US 66511 96 B1	<input checked="" type="checkbox"/>	Semiconductor device having test mode entry circuit	714/724
21	US 66314 63 B1	<input checked="" type="checkbox"/>	Method and apparatus for patching problematic instructions in a microprocessor using software interrupts	712/227
22	US 66178 42 B2	<input type="checkbox"/>	Semiconductor device testing method and system employing trace data	324/158 .1
23	US 65775 50 B2	<input checked="" type="checkbox"/>	Control circuit and semiconductor memory device	365/222
24	US 65747 27 B1	<input checked="" type="checkbox"/>	Method and apparatus for instruction sampling for performance monitoring and debug	712/227
25	US 65667 60 B1	<input checked="" type="checkbox"/>	Semiconductor storage device having memory chips in a stacked structure	257/777
26	US 65529 55 B1	<input checked="" type="checkbox"/>	Semiconductor memory device with reduced power consumption	365/233
27	US 65499 91 B1	<input checked="" type="checkbox"/>	Pipelined SDRAM memory controller to optimize bus utilization	711/158
28	US 65494 75 B2	<input type="checkbox"/>	Semiconductor memory device and information device	365/189 .12
29	US 65395 02 B1	<input checked="" type="checkbox"/>	Method and apparatus for identifying instructions for performance monitoring in a microprocessor	714/47
30	US 65047 89 B2	<input type="checkbox"/>	Semiconductor memory device	365/233
31	US 64929 92 B2	<input checked="" type="checkbox"/>	Graphic pattern processing apparatus	345/568
32	US 64876 29 B1	<input checked="" type="checkbox"/>	Semiconductor memory for operation in a plurality of operational modes	711/104
33	US 64635 18 B1	<input checked="" type="checkbox"/>	Generation of memory addresses for accessing a memory utilizing scheme registers	711/220
34	US 64532 78 B1	<input checked="" type="checkbox"/>	Flexible implementation of a system management mode (SMM) in a processor	703/27
35	US 64265 60 B1	<input checked="" type="checkbox"/>	Semiconductor device and memory module	257/777
36	US 64250 47 B1	<input type="checkbox"/>	Process containing address decoders suited to improvements in clock speed	711/101
37	US 64145 30 B2	<input checked="" type="checkbox"/>	Semiconductor integrated circuit device, semiconductor memory system and clock synchronous circuit	327/269
38	US 63817 20 B1	<input checked="" type="checkbox"/>	Test circuit and method for system logic	714/727
39	US 63811 90 B1	<input checked="" type="checkbox"/>	Semiconductor memory device in which use of cache can be selected	365/230 .03
40	US 63361 78 B1	<input checked="" type="checkbox"/>	RISC86 instruction set	712/23



	Docum ent ID	U	Title	Current OR
41	US 62928 48 B1	<input checked="" type="checkbox"/>	Computing system adapter card for supporting legacy and plug and play configurations	710/8
42	US 62085 63 B1	<input checked="" type="checkbox"/>	Semiconductor memory device which continuously performs read/write operations with short access time	365/189 .05
43	US 61417 42 A	<input checked="" type="checkbox"/>	Method for reducing number of bits used in storage of instruction address pointer values	711/220
44	US 60932 13 A	<input checked="" type="checkbox"/>	Flexible implementation of a system management mode (SMM) in a processor	703/27
45	US 60853 14 A	<input checked="" type="checkbox"/>	Central processing unit including APX and DSP cores and including selectable APX and DSP execution modes	712/213
46	US 60818 86 A	<input checked="" type="checkbox"/>	Holding mechanism for changing operation modes in a pipelined computer	712/229
47	US 60322 47 A	<input checked="" type="checkbox"/>	Central processing unit including APX and DSP cores which receives and processes APX and DSP instructions	712/35
48	US 60147 14 A	<input checked="" type="checkbox"/>	Adapter card system including for supporting multiple configurations using mapping bit	710/8
49	US 59915 31 A	<input checked="" type="checkbox"/>	Scalable width vector processor architecture for efficient emulation	703/26
50	US 59739 88 A	<input checked="" type="checkbox"/>	Semiconductor memory device having circuit for monitoring set value of mode register	365/230 .08
51	US 59266 42 A	<input checked="" type="checkbox"/>	RISC86 instruction set	712/1
52	US 59251 23 A	<input checked="" type="checkbox"/>	Processor for executing instruction sets received from a network or from a local memory	712/212
53	US 59207 13 A	<input checked="" type="checkbox"/>	Instruction decoder including two-way emulation code branching	712/236
54	US 59095 67 A	<input checked="" type="checkbox"/>	Apparatus and method for native mode processing in a RISC-based CISC processor	712/208
55	US 58939 27 A	<input checked="" type="checkbox"/>	Memory device having programmable device width, method of programming, and method of setting device width for memory device	711/171
56	US 58549 13 A	<input checked="" type="checkbox"/>	Microprocessor with an architecture mode control capable of supporting extensions of two distinct instruction-set architectures	712/210
57	US 58524 28 A	<input checked="" type="checkbox"/>	Display driving device	345/100
58	US 58190 56 A	<input checked="" type="checkbox"/>	Instruction buffer organization method and system	712/204
59	US 58092 73 A	<input checked="" type="checkbox"/>	Instruction predecode and multiple instruction decode	712/210
60	US 58023 60 A	<input checked="" type="checkbox"/>	Digital microprocessor device having dynamically selectable instruction execution intervals	712/229
61	US 57940 63 A	<input checked="" type="checkbox"/>	Instruction decoder including emulation using indirect specifiers	712/23
62	US 57937 75 A	<input checked="" type="checkbox"/>	Low voltage test mode operation enable scheme with hardware safeguard	714/724
63	US 57817 50 A	<input checked="" type="checkbox"/>	Dual-instruction-set architecture CPU with hidden software emulation mode	712/209

	Docum ent ID	U	Title	Current OR
64	US 57614 90 A	<input type="checkbox"/>	Changing the meaning of a pre-decode bit in a cache memory depending on branch prediction mode	712/239
65	US 57036 16 A	<input checked="" type="checkbox"/>	Display driving device	345/98
66	US 56637 45 A	<input checked="" type="checkbox"/>	Display driving device	345/98
67	US 56361 73 A	<input checked="" type="checkbox"/>	Auto-precharge during bank selection	365/230 .03
68	US 56301 61 A	<input checked="" type="checkbox"/>	Serial-parallel digital signal processor	712/36
69	US 55600 36 A	<input checked="" type="checkbox"/>	Data processing having incircuit emulation function	712/227
70	US 55308 04 A	<input checked="" type="checkbox"/>	Superscalar processor with plural pipelined execution units each unit selectively having both normal and debug modes	714/30
71	US 55069 70 A	<input type="checkbox"/>	Bus arbitrator circuit	710/113
72	US 54127 84 A	<input type="checkbox"/>	Apparatus for parallelizing serial instruction sequences and creating entry points into parallelized instruction sequences at places other than beginning of particular parallelized instruction sequence	712/245
73	US 54086 58 A	<input type="checkbox"/>	Self-scheduling parallel computer system and method	712/216
74	US 53964 98 A	<input checked="" type="checkbox"/>	Integrated circuit with peripheral test controller	714/703
75	US 53476 39 A	<input type="checkbox"/>	Self-parallelizing computer system and method	712/203
76	US 52805 93 A	<input checked="" type="checkbox"/>	Computer system permitting switching between architected and interpretation instructions in a pipeline by enabling pipeline drain	712/208
77	US 52261 64 A	<input checked="" type="checkbox"/>	Millicode register management and pipeline reset	712/209
78	US 51670 26 A	<input checked="" type="checkbox"/>	Simultaneously or sequentially decoding multiple specifiers of a variable length pipeline instruction based on detection of modified value of specifier registers	712/210
79	US 51485 28 A	<input checked="" type="checkbox"/>	Method and apparatus for simultaneously decoding three operands in a variable length instruction when one of the operands is also of variable length	712/210
80	US 51426 33 A	<input checked="" type="checkbox"/>	Preprocessing implied specifiers in a pipelined processor	712/225
81	US 51290 79 A	<input checked="" type="checkbox"/>	Computer system having subinstruction surveillance capability	712/211
82	US 51230 96 A	<input checked="" type="checkbox"/>	Data processor with addressing mode decoding function	712/212
83	US 50310 96 A	<input checked="" type="checkbox"/>	Method and apparatus for compressing the execution time of an instruction stream executing in a pipelined processor	711/169
84	US 45614 43 A	<input checked="" type="checkbox"/>	Coherent inductive communications link for biomedical applications	607/31
85	US 44146 22 A	<input type="checkbox"/>	Addressing system for a computer, including a mode register	711/215

	Docum ent ID	U	Title	Current OR
86	US 43441 29 A	<input checked="" type="checkbox"/>	Data processor system capable of providing both a computer mode and a sequencer mode of operation	712/229
87	US 41998 10 A	<input checked="" type="checkbox"/>	Radiation hardened register file	714/15
88	US 41077 81 A	<input checked="" type="checkbox"/>	Electronic calculator or microprocessor with indirect addressing	708/100
89	US 40842 35 A	<input checked="" type="checkbox"/>	Emulation apparatus	703/26
90	US 38184 60 A	<input checked="" type="checkbox"/>	EXTENDED MAIN MEMORY ADDRESSING APPARATUS	711/2
91	US 35771 90 A	<input type="checkbox"/>	APPARATUS IN A DIGITAL COMPUTER FOR ALLOWING THE SKIPPING OF PREDETERMINED INSTRUCTIONS IN A SEQUENCE OF INSTRUCTIONS, IN RESPONSE TO THE OCCURRENCE OF CERTAIN CONDITIONS	712/226

	L #	Hits	Search Text	DBs
1	L1	611	decod\$3 near10 (condition\$3 near5 (instruction command) not (branch adj instruction))	USPAT; US-PGPUB
2	L2	613	decod\$3 near10 (conditional near5 (instruction command) )	USPAT; US-PGPUB
3	L3	71	decod\$3 near10 (conditional adj (instruction command) )	USPAT; US-PGPUB
4	L4	46	3 near30 (memory register storage)	USPAT; US-PGPUB
5	L5	21	1 near10 (depend\$3 result) near30 (memory register storage)	USPAT; US-PGPUB
6	L6	1921	decod\$3 near10 (instruction command) near10 (modif\$6 chang\$3 alter\$3)	USPAT; US-PGPUB
7	L7	750	6 near20 (register memory storage flag)	USPAT; US-PGPUB
8	L9	58	7 near10 (result meaning depend\$3 )	USPAT; US-PGPUB
9	L8	72	7 near10 (result meaning depend\$3 based)	USPAT; US-PGPUB

	Docum ent ID	U	Title	Current OR
1	US 20030 22600 2 A1	<input type="checkbox"/>	Devices, systems and methods for conditional instructions notice	712/234
2	US 20030 10579 3 A1	<input type="checkbox"/>	Long instruction word controlling plural independent processor operations	708/625
3	US 20020 04043 0 A1	<input type="checkbox"/>	Microcontroller	712/234
4	US 66812 80 B1	<input type="checkbox"/>	Interrupt control apparatus and method separately holding respective operation information of a processor preceding a normal or a break interrupt	710/261
5	US 65164 07 B1	<input type="checkbox"/>	Information processor	712/226
6	US 64272 05 B1	<input type="checkbox"/>	Digital signal processor and processor reducing the number of instructions upon processing condition execution instructions	712/226
7	US 63453 55 B1	<input type="checkbox"/>	Method and apparatus for distributing commands to a plurality of circuit blocks	712/215
8	US 63341 81 B1	<input type="checkbox"/>	DSP with wait state registers having at least two portions	712/38
9	US 63112 64 B1	<input type="checkbox"/>	Digital signal processor with wait state register	712/38
10	US 62634 19 B1	<input type="checkbox"/>	Integrated circuit with wait state registers	712/38
11	US 62634 18 B1	<input type="checkbox"/>	Process of operating a microprocessor to use wait state numbers	712/38
12	US 62533 07 B1	<input type="checkbox"/>	Data processing device with mask and status bits for selecting a set of status conditions	712/209
13	US 62498 60 B1	<input type="checkbox"/>	System with wait state registers	712/38
14	US 62498 59 B1	<input type="checkbox"/>	IC with wait state registers	712/38
15	US 62471 11 B1	<input type="checkbox"/>	System with wait state register	712/38
16	US 62438 01 B1	<input type="checkbox"/>	System with wait state registers	712/38
17	US 62405 05 B1	<input type="checkbox"/>	System with wait state registers	712/38
18	US 62405 04 B1	<input type="checkbox"/>	Process of operating a microprocessor to change wait states	712/38
19	US 61345 78 A	<input type="checkbox"/>	Data processing device and method of operation with context switching	718/100
20	US 60853 36 A	<input type="checkbox"/>	Data processing devices, systems and methods with mode driven stops	714/30
21	US 60527 76 A	<input type="checkbox"/>	Branch operation system where instructions are queued until preparations is ascertained to be completed and branch distance is considered as an execution condition	712/233
22	US 59464 83 A	<input type="checkbox"/>	Devices, systems and methods for conditional instructions	712/223

	Docum ent ID	U	Title	Current OR
23	US 59077 14 A	<input type="checkbox"/>	Method for pipelined data processing with conditioning instructions for controlling execution of instructions without pipeline flushing	712/23
24	US 58290 54 A	<input type="checkbox"/>	Devices and systems with parallel logic unit operable on data memory locations	711/202
25	US 58285 77 A	<input type="checkbox"/>	Devices and systems with protective terminal configuration, and methods	716/4
26	US 57778 85 A	<input type="checkbox"/>	Devices and systems with protective terminal configuration, and methods	716/1
27	US 57242 48 A	<input type="checkbox"/>	Devices and systems with protective terminal configuration, and methods	716/4
28	US 56873 39 A	<input type="checkbox"/>	Pre-reading and pre-decoding of instructions of a microprocessor within single cycle	712/207
29	US 56529 10 A	<input type="checkbox"/>	Devices and systems with conditional instructions	712/218
30	US 56175 74 A	<input type="checkbox"/>	Devices, systems and methods for conditional instructions	712/200
31	US 55862 75 A	<input type="checkbox"/>	Devices and systems with parallel logic unit operable on data memory locations, and methods	712/223
32	US 55837 67 A	<input type="checkbox"/>	Devices and systems with parallel logic unit, and methods notice	701/1
33	US 55794 97 A	<input type="checkbox"/>	Devices and systems with parallel logic unit, and methods	375/222
34	US 55792 18 A	<input type="checkbox"/>	Devices and systems with parallel logic unit, and methods	700/1
35	US 55509 93 A	<input type="checkbox"/>	Data processor with sets of two registers where both registers receive identical information and when context changes in one register the other register remains unchanged	712/229
36	US 55091 29 A	<input type="checkbox"/>	Long instruction word controlling plural independent processor operations	712/203
37	US 53831 96 A	<input type="checkbox"/>	SONET signal generating apparatus and method	714/712
38	US 53496 87 A	<input type="checkbox"/>	Speech recognition system having first and second registers enabling both to concurrently receive identical information in one context and disabling one to retain the information in a next context	704/231
39	US 53197 92 A	<input type="checkbox"/>	Modem having first and second registers enabling both to concurrently receive identical information in one context and disabling one to retain the information in a next context	712/228
40	US 53197 89 A	<input type="checkbox"/>	Electromechanical apparatus having first and second registers enabling both to concurrently receive identical information in one context and disabling one to retain the information in a next context	712/228
41	US 53136 48 A	<input type="checkbox"/>	Signal processing apparatus having first and second registers enabling both to concurrently receive identical information in one context and disabling one to retain the information in a next context	712/228
42	US 51558 12 A	<input type="checkbox"/>	Devices and method for generating and using systems, software waitstates on address boundaries in data processing	710/59
43	US 51426 77 A	<input type="checkbox"/>	Context switching devices, systems and methods	718/108
44	US 50724 18 A	<input type="checkbox"/>	Series maxium/minimum function computing devices, systems and methods	708/207

	Docum ent ID	U	Title	Current OR
45	US 45983 58 A	<input type="checkbox"/>	Pipelined digital signal processor using a common data and control bus	712/35
46	US 45396 35 A	<input type="checkbox"/>	Pipelined digital processor arranged for conditional operation	712/234

	Docum ent ID	U	Title	Current OR
1	US 20030 18258 9 A1	<input type="checkbox"/>	Instruction conversion apparatus and instruction conversion method providing power control information, program and circuit for implementing the instruction conversion, and microprocessor for executing the converted instruction	713/300
2	US 20020 04043 0 A1	<input type="checkbox"/>	Microcontroller	712/234
3	US 20020 03572 4 A1	<input type="checkbox"/>	Data rate conversion	725/1
4	US 66788 19 B1	<input type="checkbox"/>	Pipeline microprocessor with conditional jump in one clock cycle	712/219
5	US 64272 05 B1	<input type="checkbox"/>	Digital signal processor and processor reducing the number of instructions upon processing condition execution instructions	712/226
6	US 63269 99 B1	<input type="checkbox"/>	Data rate conversion	348/441
7	US 60264 80 A	<input type="checkbox"/>	Processor having bug avoidance function and method for avoiding bug in processor	712/37
8	US 59580 48 A	<input type="checkbox"/>	Architectural support for software pipelining of nested loops	712/241
9	US 57649 41 A	<input type="checkbox"/>	Operating circuit and method for processing signals in ADPCM system	712/209
10	US 52533 49 A	<input type="checkbox"/>	Decreasing processing time for type 1 dyadic instructions	712/223
11	US 49597 80 A	<input type="checkbox"/>	Microprogram processor with logic circuitry for combining signals from a microcode decoder and an instruction code decoder to produce a memory access signal	712/212
12	US 47195 63 A	<input type="checkbox"/>	Data transmission control device for controlling transfer of large amounts of data between two memory units	711/165
13	US 45983 58 A	<input type="checkbox"/>	Pipelined digital signal processor using a common data and control bus	712/35
14	US 45396 35 A	<input type="checkbox"/>	Pipelined digital processor arranged for conditional operation	712/234
15	US 42518 59 A	<input type="checkbox"/>	Data processing system with an enhanced pipeline control	712/219
16	US 40259 02 A	<input type="checkbox"/>	General purpose sequence controller	700/18
17	US 39097 99 A	<input type="checkbox"/>	Microprogrammable peripheral processing system	712/234
18	US 38497 65 A	<input type="checkbox"/>	PROGRAMMABLE LOGIC CONTROLLER	712/246
19	US 38326 96 A	<input type="checkbox"/>	GENERAL PURPOSE SEQUENCE CONTROLLER	700/9
20	US 37365 66 A	<input type="checkbox"/>	CENTRAL PROCESSING UNIT WITH HARDWARE CONTROLLED CHECKPOINT AND RETRY FACILITIES	714/15
21	US 35789 18 A	<input type="checkbox"/>	COMPUTER CONTROLLED SWITCHING SYSTEM USING FLIP-FLOPS FOR CONTROL OF REPETITIVE OPERATIONS	379/280



	Docum ent ID	U	Title	Current OR
1	US 20040 00321 4 A1	<input type="checkbox"/>	Instruction control method and processor	712/234
2	US 20040 00320 7 A1	<input type="checkbox"/>	Program counter control method and processor	712/218
3	US 20030 20465 2 A1	<input type="checkbox"/>	Data transfer control device, electronic equipment and data transfer control method	710/33
4	US 20030 14475 5 A1	<input type="checkbox"/>	Method for processing and reproducing audio signal at desired sound quality, reduced data volume or adjusted output level, apparatus for processing audio signal with sound quality control information or test tone signal or at reduced data volume, recording medium for recording audio signal with sound quality control information or test tone signal or at reduced data volume, and apparatus for reproducing audio signal at desired sound quality, reduced data volume or adjusted output level	700/94
5	US 20030 09365 2 A1	<input type="checkbox"/>	Operand file using pointers and reference counters and a method of use	712/217
6	US 20030 03351 1 A1	<input type="checkbox"/>	Processor having multiple program counters and trace buffers outside an execution pipeline	712/235
7	US 20030 02634 2 A1	<input type="checkbox"/>	Decoding apparatus, decoding method, decoding program, and decoding program storage medium	375/240 .25
8	US 20030 00458 8 A1	<input type="checkbox"/>	Method for processing and reproducing audio signal at desired sound quality, reduced data volume or adjusted output level, apparatus for processing audio signal with sound quality control information or test tone signal or at reduced data volume, recording medium for recording audio signal with sound quality control information or test tone signal or at reduced data volume, and apparatus for reproducing audio signal at desired sound quality, reduced data volume or adjusted output level	700/94
9	US 20020 19445 7 A1	<input type="checkbox"/>	Memory system for ordering load and store instructions in a processor that performs out-of-order multithread execution	712/218
10	US 20020 17107 5 A1	<input type="checkbox"/>	Register setting method and semiconductor device	257/10
11	US 20020 12873 9 A1	<input type="checkbox"/>	Method for processing and reproducing audio signal at desired sound quality, reduced data volume or adjusted output level, apparatus for processing audio signal with sound quality control information or test tone signal or at reduced data volume, recording medium for recording audio signal with sound quality control information or test tone signal or at reduced data volume, and apparatus for reproducing audio signal at desired sound quality, reduced data volume or adjusted output level	700/94
12	US 20020 12381 0 A1	<input type="checkbox"/>	Method for processing and reproducing audio signal at desired sound quality, reduced data volume or adjusted output level, apparatus for processing audio signal with sound quality control information or test tone signal or at reduced data volume, recording medium for recording audio signal with sound quality control information or test tone signal or at reduced data volume, and apparatus for reproducing audio signal at desired sound quality, reduced data	700/94

	Docum ent ID	U	Title	Current OR
13	US 20010 01494 1 A1	<input type="checkbox"/>	Processor having multiple program counters and trace buffers outside an execution pipeline	712/228
14	US 66788 18 B1	<input type="checkbox"/>	Decoding next instruction of different length without length mode indicator change upon length change instruction detection	712/210
15	US 66041 93 B1	<input type="checkbox"/>	Processor in which register number translation is carried out	712/228
16	US 65606 92 B1	<input type="checkbox"/>	Data processing circuit, microcomputer, and electronic equipment	712/23
17	US 65604 97 B2	<input type="checkbox"/>	METHOD FOR PROCESSING AND REPRODUCING AUDIO SIGNAL AT DESIRED SOUND QUALITY, REDUCED DATA VOLUME OR ADJUSTED OUTPUT LEVEL, APPARATUS FOR PROCESSING AUDIO SIGNAL WITH SOUND QUALITY CONTROL INFORMATION OR TEST TONE SIGNAL OR AT REDUCED DATA VOLUME, RECORDING MEDIUM FOR RECORDING AUDIO SIGNAL WITH SOUND QUALITY CONTROL INFORMATION OR TEST TONE SIGNAL OR AT REDUCED DATA VOLUME, AND APPARATUS FOR REPRODUCING AUDIO SIGNAL AT DESIRED SOUND QUALITY, REDUCED DATA VOLUME OR ADJUSTED OUTPUT LEVEL	700/94
18	US 65499 59 B1	<input type="checkbox"/>	Detecting modification to computer memory by a DMA device	710/22
19	US 65359 84 B1	<input type="checkbox"/>	Power reduction for multiple-instruction-word processors with proxy NOP instructions	713/320
20	US 64938 20 B2	<input type="checkbox"/>	Processor having multiple program counters and trace buffers outside an execution pipeline	712/235
21	US 64635 22 B1	<input type="checkbox"/>	Memory system for ordering load and store instructions in a processor that performs multithread execution	712/216
22	US 64569 66 B1	<input type="checkbox"/>	Apparatus and method for decoding audio signal coding in a DSR system having memory	704/212
23	US 64427 01 B1	<input type="checkbox"/>	Power saving by disabling memory block access for aligned NOP slots during fetch of multiple instruction words	713/324
24	US 64272 05 B1	<input type="checkbox"/>	Digital signal processor and processor reducing the number of instructions upon processing condition execution instructions	712/226
25	US 63973 79 B1	<input type="checkbox"/>	Recording in a program execution profile references to a memory-mapped active device	717/140
26	US 63780 61 B1	<input type="checkbox"/>	Apparatus for issuing instructions and reissuing a previous instructions by recirculating using the delay circuit	712/200
27	US 63778 62 B1	<input type="checkbox"/>	Method for processing and reproducing audio signal	700/94
28	US 63082 61 B1	<input type="checkbox"/>	Computer system having an instruction for probing memory latency	712/219
29	US 62405 09 B1	<input type="checkbox"/>	Out-of-pipeline trace buffer for holding instructions that may be re-executed following misspeculation	712/228
30	US 62055 34 B1	<input type="checkbox"/>	Apparatus and method for processing data with a plurality of flag groups	712/32
31	US 61822 10 B1	<input type="checkbox"/>	Processor having multiple program counters and trace buffers outside an execution pipeline	712/235
32	US 61700 82 B1	<input type="checkbox"/>	Taking corrective action in computer programs during instruction processing	717/127

	Docum ent ID	U	Title	Current OR
33	US 61579 97 A	<input type="checkbox"/>	Processor and information processing apparatus with a reconfigurable circuit	712/226
34	US 60818 86 A	<input type="checkbox"/>	Holding mechanism for changing operation modes in a pipelined computer	712/229
35	US 60732 49 A	<input type="checkbox"/>	Information processing system	714/4
36	US 60264 80 A	<input type="checkbox"/>	Processor having bug avoidance function and method for avoiding bug in processor	712/37
37	US 60121 41 A	<input type="checkbox"/>	Apparatus for detecting and executing traps in a superscalar processor	712/244
38	US 59918 68 A	<input type="checkbox"/>	Apparatus and method for processing data with a plurality of flag groups	712/32
39	US 59915 31 A	<input type="checkbox"/>	Scalable width vector processor architecture for efficient emulation	703/26
40	US 59179 47 A	<input type="checkbox"/>	Image processing method and apparatus permitting use of PDL in compression memory	382/232
41	US 58986 21 A	<input type="checkbox"/>	Batch erasable single chip nonvolatile memory device and erasing method therefor	365/185 .33
42	US 58954 97 A	<input type="checkbox"/>	Microprocessor with pipelining, memory size evaluation, micro-op code and tags	711/169
43	US 58929 23 A	<input type="checkbox"/>	Parallel computer system using properties of messages to route them through an interconnect network and to select virtual channel circuits therewithin	709/239
44	US 58729 64 A	<input type="checkbox"/>	Comparison operating unit and graphic operating system	712/234
45	US 58356 97 A	<input type="checkbox"/>	Information processing system	714/11
46	US 58023 38 A	<input type="checkbox"/>	Method of self-parallelizing and self-parallelizing multiprocessor using the method	712/217
47	US 57614 90 A	<input type="checkbox"/>	Changing the meaning of a pre-decode bit in a cache memory depending on branch prediction mode	712/239
48	US 56921 70 A	<input type="checkbox"/>	Apparatus for detecting and executing traps in a superscalar processor	712/244
49	US 56492 29 A	<input type="checkbox"/>	Pipeline data processor with arithmetic/logic unit capable of performing different kinds of calculations in a pipeline stage	712/24
50	US 56320 23 A	<input type="checkbox"/>	Superscalar microprocessor including flag operand renaming and forwarding apparatus	712/218
51	US 55983 68 A	<input type="checkbox"/>	Batch erasable nonvolatile memory device and erasing method	365/185 .01
52	US 55111 72 A	<input type="checkbox"/>	Speculative execution processor	712/235
53	US 55069 70 A	<input type="checkbox"/>	Bus arbitrator circuit	710/113
54	US 54815 49 A	<input type="checkbox"/>	Apparatus for testing an integrated circuit in which an input test pattern can be changed with an selected application timing	714/744
55	US 54505 55 A	<input type="checkbox"/>	Register logging in pipelined computer using register log queue of register content changes and base queue of register log queue pointers for respective instructions	712/228

	Docum ent ID	U	Title	Current OR
56	US 54189 17 A	<input type="checkbox"/>	Method and apparatus for controlling conditional branch instructions for a pipeline type data processing apparatus	712/234
57	US 54127 84 A	<input type="checkbox"/>	Apparatus for parallelizing serial instruction sequences and creating entry points into parallelized instruction sequences at places other than beginning of particular parallelized instruction sequence	712/245
58	US 54086 58 A	<input type="checkbox"/>	Self-scheduling parallel computer system and method	712/216
59	US 54045 54 A	<input type="checkbox"/>	Information processing system which converts specific instruction codes to non-user defined instruction codes	712/226
60	US 53966 03 A	<input type="checkbox"/>	Data processor having resources and execution start control for starting execution of succeeding instruction in resource before completion of preceding instruction	712/216
61	US 53496 71 A	<input type="checkbox"/>	Microprocessor system generating instruction fetch addresses at high speed	712/234
62	US 53476 39 A	<input type="checkbox"/>	Self-parallelizing computer system and method	712/203
63	US 53332 88 A	<input type="checkbox"/>	Effective address pre-calculation type pipelined microprocessor	711/214
64	US 51670 26 A	<input type="checkbox"/>	Simultaneously or sequentially decoding multiple specifiers of a variable length pipeline instruction based on detection of modified value of specifier registers	712/210
65	US 49822 83 A	<input type="checkbox"/>	Line-sequential pyramid processing of a plurality of raster-scanned image variables	375/240 .12
66	US 48315 15 A	<input type="checkbox"/>	Information processing apparatus for determining sequence of parallel executing instructions in response to storage requirements thereof	712/217
67	US 47440 43 A	<input type="checkbox"/>	Data processor execution unit which receives data with reduced instruction overhead	708/490
68	US 44569 94 A	<input type="checkbox"/>	Remote simulation by remote control from a computer desk	714/33
69	US 44146 22 A	<input type="checkbox"/>	Addressing system for a computer, including a mode register	711/215
70	US 43608 91 A	<input type="checkbox"/>	Address and data interface unit	712/208
71	US 41387 19 A	<input type="checkbox"/>	Automatic writing systems and methods of word processing therefor	358/1.1 8
72	US 37365 66 A	<input type="checkbox"/>	CENTRAL PROCESSING UNIT WITH HARDWARE CONTROLLED CHECKPOINT AND RETRY FACILITIES	714/15